

TOTAL 5 QUESTIONS

NOTE: State your assumptions clearly

- ✓ Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat and labeled properly. NO MARKS for unnecessary theoretical explanation.
- ✓ Although your answers are important, your REASONS for giving those answers are even more important. Please, explain what you are doing and why. So, justify your answers

Given $g_{inv}=1$, $p_{inv}=1$, for standard CMOS inverter.

Common data: Use the following common data if not mentioned specifically in the question

For $0.25\mu\text{m}$ Technology node --

- Take $V_{dd}=2.5\text{ V}$, $|V_{tn}|=|V_{tp}|=0.5\text{ V}$, $W_{\min}=L_{\min}=0.5\ \mu\text{m}$, $\gamma=0$, $u_n C_{ox}=120\ \mu\text{A}/\text{V}^2$, $u_p C_{ox}=60\ \mu\text{A}/\text{V}^2$,
- Velocity of electromagnetic wave in wire = $15\ \text{cm}/\text{nsec}$
- On-resistances of NMOS and PMOS transistors equals $[20\ \text{k}\ \Omega/(W/L)]$ and $[40\ \text{k}\ \Omega/(W/L)]$, respectively
- Clock signal has 50% duty cycle.
- Wire resistance per unit length (for wire width= $1\ \mu\text{m}$)= $0.05\ \text{ohm}/\ \mu\text{m}$, Wire capacitance per unit length (for wire width= $1\ \mu\text{m}$)= $2\ \text{femto F}/\ \mu\text{m}$

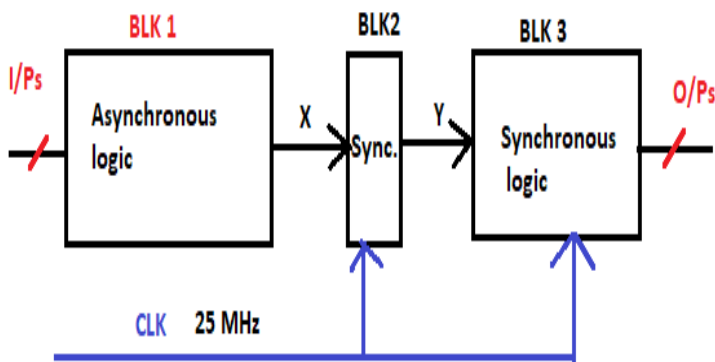


Fig. 1

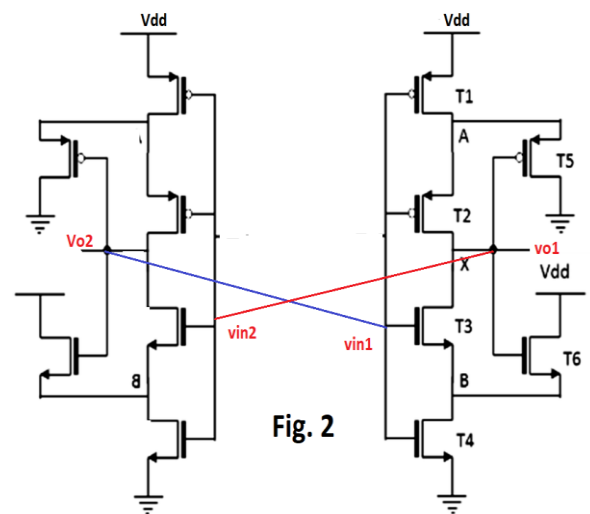


Fig. 2

Q1. Consider Fig. 1. . Given signal rise time $t_{\text{rise}} = 20\text{ ns}$

- Blk-1 is a 4-phase pipeline with 'done' signal with maximum cycle time= $1\ \mu\text{ sec}$
- Blk-2 is a 4-stage cascaded synchronizer.
- Blk-3 is positive edge triggered clocked pipeline, with Clk frequency = $25\ \text{MHz}$
- D-FF has $T_{\text{setup}}=T_{\text{hold}}=T_{\text{c-q}}=5\ \text{n-sec}$,
- Bi-stable element (cross coupled inverter) has time constant- $=\tau = 4\text{ nano Sec}$

- Determine Mean time between failure (MTBF) of BLK-2 (in years).
- Re-estimate MTBF of BLK-2 If clk has a positive skew of 100 pS in Fig. 2, (in years).
- Re-estimate MTBF of BLK-2 , If only first two stages of Blk-2 are operated with frequency of Blk-1 in Fig. 2 (in years).
- In part (a) , the bistable element of each stage is replaced by cross coupled Schmitt trigger circuit. (Fig. 2) . It has upper threshold = 1V and lower threshold = 0.5V . $\tau = 5nS$. Re-estimate MTBF (in years).

(PTO)

[8 marks]

Q2. For BLK-1 in Fig. 1-- the synchronous logic design of BLK 1 is shown in Fig. 3. Assume $1 C_g = W_{min} L_{min} C_{ox}$

Cox

- Sketch and lable the entire schematic of longest CLB data path/s i.e (i1, i2----i7 to O1/ O2).
- Determine logical effort of each stage in part (a) in each data path/s
- Hence determine path effort 'F' of each data path/s
- Determine the minimum delay of path consisting of domino gates without changing number of stages. In the path.

[10 marks]

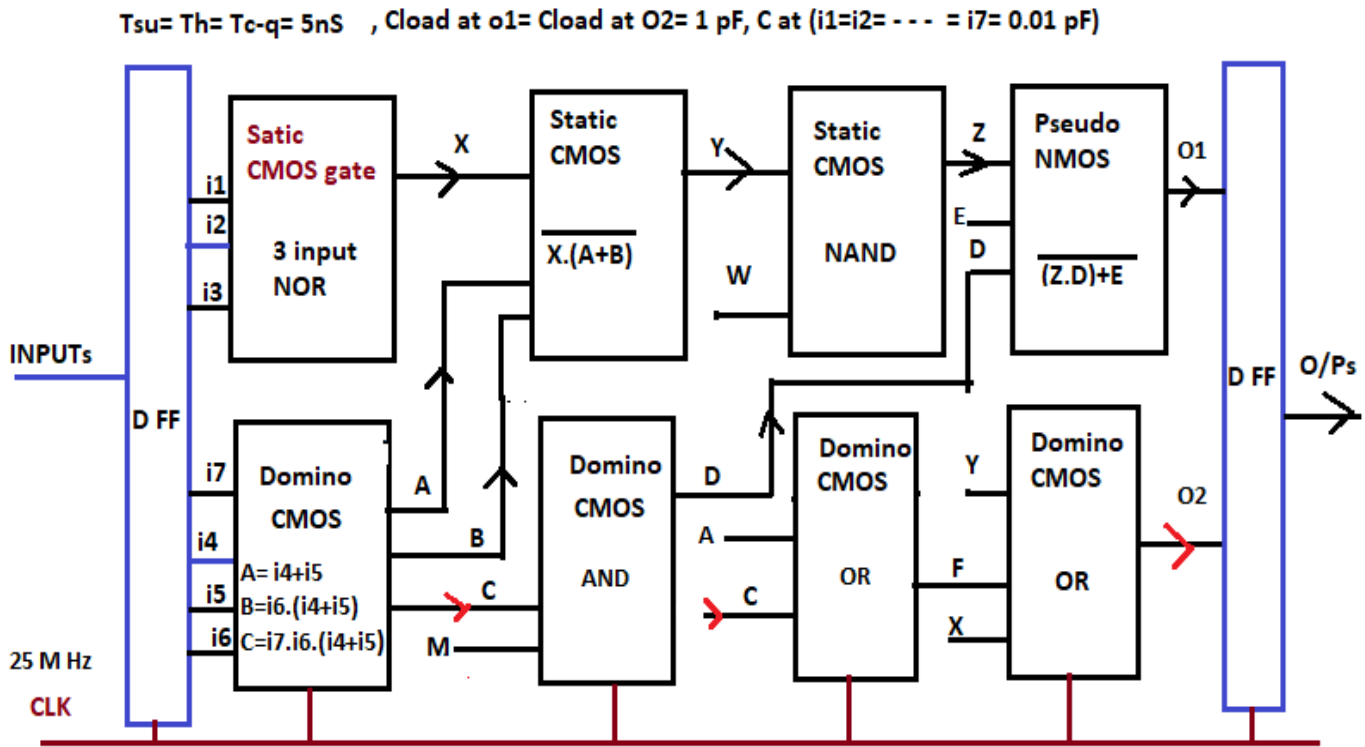


FIG. 3

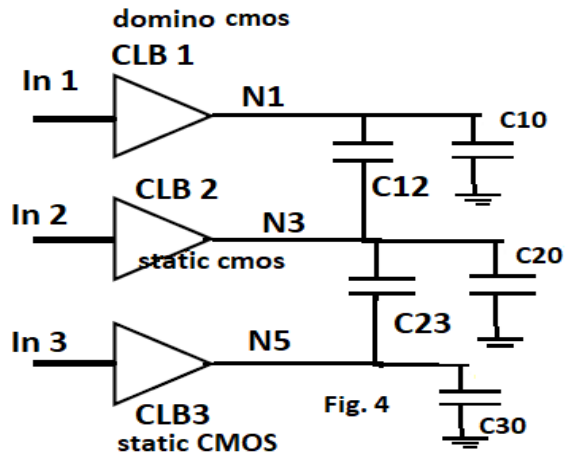
PTO

Q3. Consider Fig. 4 with nodes N1, N2, N3 are in vicinity of each other. Given $C_{10}=C_{20}=C_{30}$, and coupling capacitors $C_{23}=C_{12}= (0.25)C_{20}$,

Determine the max. voltage level ----

- at node N3 if node N3 is initially charged to V_{dd} , and then only N5 switches from V_{dd} to 0.
- at node N1 if node N1 is initially precharged to V_{dd} , and then both N3, and N5 switches from V_{dd} to 0.

[5 marks]

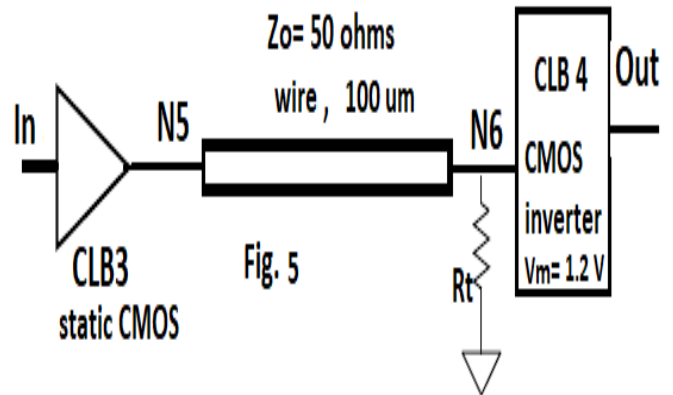


Q4. Consider Fig. 5, showing a data paths on an IC operating at 1 GHz.

Each wire / trace is **100 um long** with **20 nano-H inductance** , **2 nano-F capacitance**),

Assume loss less behavior.

- Determine termination resistance (R_t) required at nodes (N6) for incidence wave switching. Assume R_{out} of CLB3 is 50 ohms
- Now, impedances at nodes N5, and N6 changes to 60 ohms due to PVT variations . Hence, Sketch and label the lattice diagram for (rising step) signal propagation through wire.. Now find the total propagation delay from N5 to N6. Assume **$C_6= 0.1$ pF** is the input capacitance of CLB4



[6 marks]

Q5. Answer the following with proper justification/ calculation----

- Consider wire (N5 to N6) in Fig. 5, having length **100 um long** with **20 nano H inductance** , **2 nano F capacitance**), Determine the propagation delay through wire using distributed RC approach.
- Sketch and label segmented break before make pulse transmitter driver for Fig. 5
- In Fig. 5, for incidence wave switching , design thevenin termination resistance (R_t) and termination voltage V_t required at nodes (N6).
- In Fig 3, determine optimum number of stages for data path consisting of only static cmos gates..
- Now in Fig. 4, determine the net capacitive load appearing at node N3 , if N1 switches from 0 to V_{dd} , and node N3 switches from V_{dd} to 0 . (hint--- use principle of superposition)

[10 marks]

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