BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, RAJASTHAN

I SEMESTER, 2022-2023

MIDSEM TEST CLOSED BOOK (4 Nov. 2022)

MEL G623 ADVANCED VLSI DESIGN

TIME-90 MTS. MAX. MARKS=25

NOTE: Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat. NO MARKS for unnecessary theoretical explanation. Justify your answers

Vdd=3.3 V, $|V_{tn}|= |V_{tp}|= 0.7V$, $W_{min}=L_{min}= 0.5$ um, $u_nC_{ox}= 120$ uA/ V^2, $u_pC_{ox}= 60$ uA/ V^2

Rnmos= $\frac{15kohm}{(W/L)}$.

For standard CMOS inverter, g=1, p=1, tphl= tplh, 1 $C_{gmin}= W_{min}\, L_{min}\, C_{ox}$

Q1. Consider the circuit of Fig. 1

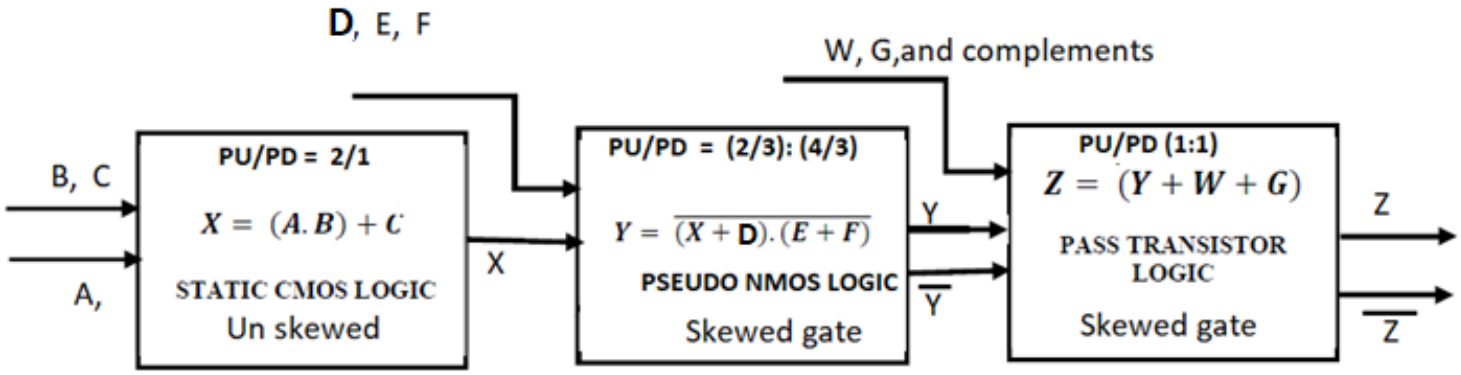

Fig. 1

a) Sketch and label the complete schematic of Fig. 1

b) Estimate ($\bar{g}, \bar{p}$) per input per output of each stage in the critical path (A to Z).

c) Hence estimate least critical path delay A to Z. Take $C_Z = 50\ C_{gmin}$. Assume (W/L) n,eq = 1 in first stage.

[10]

Q2. Consider the clock distribution as shown in Fig. 2. Premesh driver send clock signal to H tree/s. Every H tree distributes clock signal to Grid with (16,384) intersection (destination) points. Assume

--every destination point on grid has 1fF capacitive load

-- every output of pre-mesh driveer drives a 10fF load

a) If clock signal needs to be distributed to all points on Grid, estimate the (minimum) total no. of H tree and pre-mesh drivers required.

b) Hence, Sketch and label the block level diagram to represent clock distribution on chip to achieve zero skew condition. Assume pre-mesh drivers can be placed on all four sides of grid.

c) Now in part (b) , Estimate total power consumption per cycle . Neglect power consumption at intermediate nodes of H tree and pre-mesh driver

d) If the depth of H-tree and pre-mesh driver is increased by one level, re-estimate the total no. of H-tree and pre-mesh drivers required. Neglect power consumption at intermediate nodes of H tree and pre-mesh driver. For same power consumption as obtained in part-c, how many additional destination points can be driven in total.

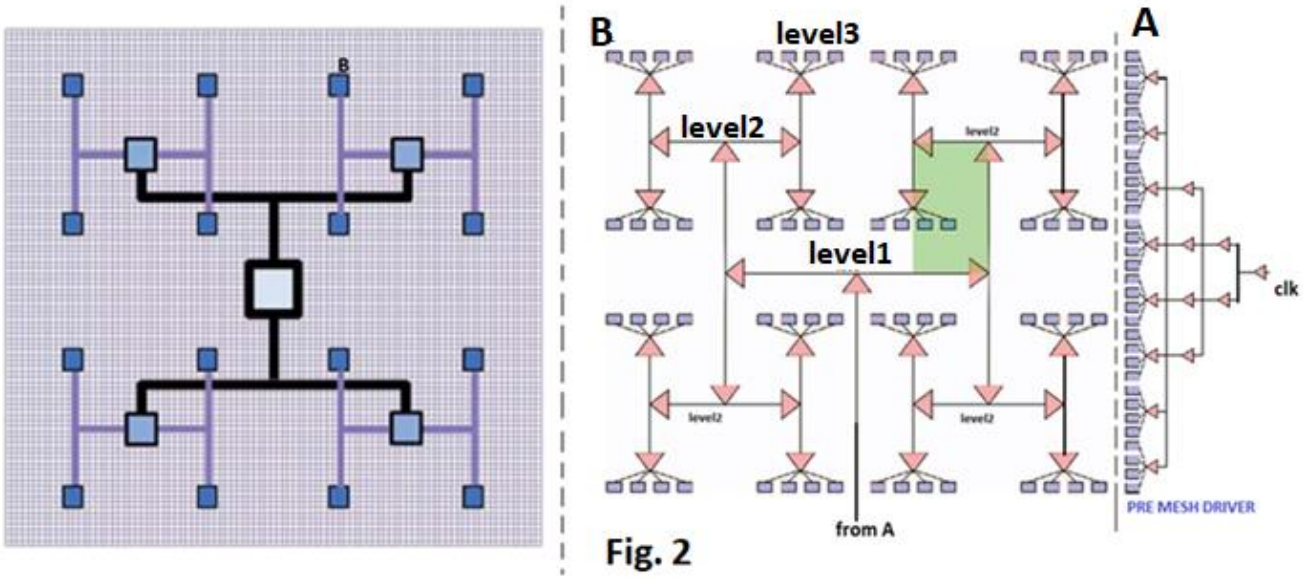

Fig. 2

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Q3. Explain the following with proper justification-----

a) In Fig. 2, If clk arrival delay can deviate by ± 10 ps at each level of pre-mesh driver and each level of H-tree due to PVT variations , estimate maximum skew that can appear between any pair of destination points.

b) Is it correct to say that a self-timed pipeline has delay insensitive property? Explain with justification.

c) Sketch and label the schematic of an edge triggered flip flop with negative setup time. Explain the circuit.

[5]

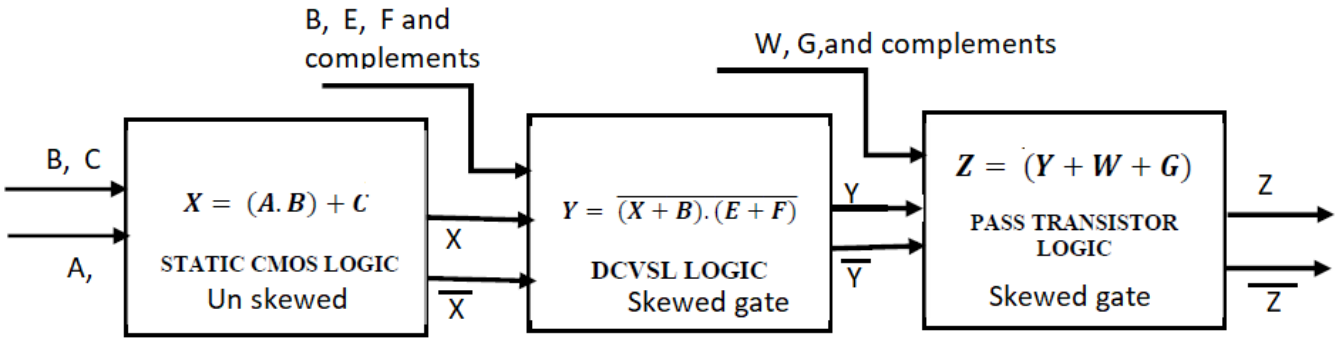
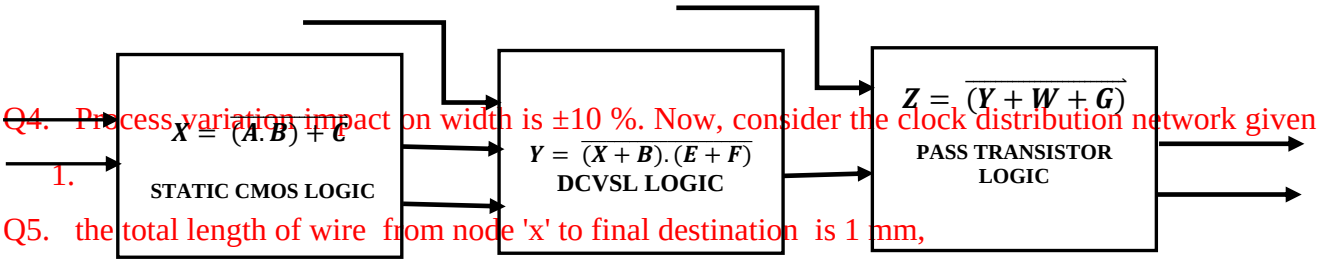


Fig. 1



Q4. Process variation impact on width is ±10 %. Now, consider the clock distribution network given in Fig. 1.

Q5. the total length of wire from node 'x' to final destination is 1 mm,

[5]

----------x----------

DYN