**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS**

Comprehensive Examination Advanced VLSI Design(MEL G623) SEMESTER-I 2022/2023

Closed Book PART A Duration: 90 Minutes Maximum marks: 20

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**Q1.** Draw and explain the operation of phase frequency detector with proper waveform taking into account all possible cases (of phase error detection and frequency error detection). **(Marks:5)**

**Q2.** Write verilog module for black cell used in adder architecture with valency as parameter. BIT GENERATE and BIT PROPAGATE are inputs. **(Marks:5)**

**Q3.** Draw optimized carry select implementation for S=4 with BIT GENERATE, BIT PROPAGATE and $C_{in}$ as inputs and SUM bits as output using OR, XOR gates, 2:1 MUX and gray cell. Such implementation is used in sparse tree architectures. **(Marks:5)**

**Q4.** Write generic script (.tcl) file used in synthesis. Also write generic constraint file. **(Marks:5)**