BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS

Comprehensive Examination Advanced VLSI Design(MEL G623) SEMESTER-I 2022/2023

Open Book PART B Duration: 90 Minutes Maximum marks: 20

Q1. For sequential circuit given below, consider all components are taken from slow_vdd1v0_basicCells.lib. T_{launch} consists of two buffers BUFX12 and BUFX12 while $T_{capture}$ consists of BUFX12 and BUFX12. Combinational logic consists of NOR2X1 (input connected to B input and is falling) followed by BUFX12. Flip-flops are DFFHQX1. Assume CLKM has clock period of 10 ns and transition time of 0.08 ns for both edges. Interconnections are ideal. Assume CK pin capacitance of flip-flop as 0.000207869 fF (library unit). Clock uncertainty is 0.05 ns.

(Marks:20)

Write **setup** and **hold** time verification report in proper format.