BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS

Midterm Test Advanced VLSI Design(MEL G623) SEMESTER-I 2022/2023

Closed Book 02.11.2022 Duration: 90 Minutes Maximum marks: 30

Q1. (a) Design Radix-4 Booth encoder and selector circuit using the control signals POS, NEG, and DOUBLE. POS is true for the multiples Y and 2Y. NEG is true for the multiples –Y and –2Y. DOUBLE is true for the multiples 2Y and –2Y. Draw the optimized circuit diagram. **(Marks:5)**

(b) Using Radix-4 modified Booth encoding scheme, show diagram (similar to dot diagram but dots replaced by actual values) of partial product addition with minimum sign bits (show actual value of sign bit used) and constants for multiplication $(128)_{10} \times (128)_{10}$ of two 8-bit unsigned numbers. **(Marks:5)**

(c) Using the binary values of given numbers in part (b), but considering them as signed numbers, show diagram of partial product addition with minimum sign bits (show actual value of sign bit used) and constants for multiplication. **(Marks:5)**

(d) Assuming index 0 for rightmost partial product addition in part (b), show the 16^{th} Vertical Compressor Slice (VCS) in a TDM multiplier with timings labeled on it. State the timing assumptions for CSA and half adder used in VCS. Also show the actual binary output values from every component used in VCS. To distinguish timing values from binary values, encircle them in the diagram. **(Marks:5)**

Q2. For a PLL following parameters are given

- VCO gain = 100 MHz/V
- Phase Detector gain = 1 V/rad
- Loop filter is low-pass filter with pole at $2\pi \times 10^6$ rad/s
- A divider of 100 placed in feedback path.

Find the transfer function of PLL. Calculate natural frequency of oscillations and damping factor for PLL. What is the boundary value of RC that can cause ringing effect? Use natural frequency calculated above for boundary value of RC. **(Marks:5)**

Q3. Draw the carry-increment adder PG network for 16 bit adder with (5, 4, 3, 2, 2) length of each group. Label the diagram properly. Compare the timing with 16 bit adder with length of each group as 4. **(Marks:5)**