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I SEMESTER, 2022-2023

MEL G623 ADVANCED VLSI DESIGN COMPREHENSIVE EXAMINATION

***OPEN BOOK* (7 December. 20223**

TIME-3 hrs. **MAX. MARKS=35**

TOTAL 5 QUESTIONS

NOTE: State your assumptions clearly

- ✓ ***Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat and labeled properly. NO MARKS for unnecessary theoretical explanation.***
- ✓ ***Although your answers are important, your REASONS for giving those answers are even more important. Please, explain what you are doing and why. So, justify your answers***

Given ginv=1, pinv=1, for standard CMOS inverter with ratio 2:1. , time-constant (250nm)=0.28 uS

***Common data**: Use the following common data **if not mentioned specifically** in the question*

For 0.25µm Technology node --

- ***Take* Vdd=2.5 V, |Vtn|= |Vtp|= 0.5V, $W_{min}=L_{min}$= 0.5 um , ϒ=0, u_nCox=120 uA/V^2, u_pCox= 60 uA/ V^2,**
- On-resistances of NMOS and PMOS transistors equals **[20 k Ω/ (*W/L*)] and [40 k Ω/(*W/L*)],** respectively
- **Clock signal has 50 % duty cycle.**
- Wire resistance per unit length (for wire width=1um)=0.05ohm/ um, Wire capacitance per unit length (for wire width=1um)= 2 femto F/um
- Transmission line characteristic impedance Zo= 50 ohms

Q1. Answer the following. justify your answers with proper reasons.

a) Typically ,a PMOS has more pronounced channel length modulation (i.e gradual transition from linear to saturation region) than NMOS. Explain which one will be more suitable as resistor.

b) A digital system operating at **2 GHz** frequency. Determine the limiting value of rise/ fall time of signal/s to avoid excessive ringing.

c) An inverter with a voltage gain of **10** and full swing **3 V** is used as a receiver driver. Determine its worst case sensitivity with **±25 % PVT variation**

d) Assuming that average length of transmission lines (of Zo= 50 ohms) in a digital system (with **0-2.5 V** signal swing operating at **1 GHz** frequency)) is **10nS**. For **25,000** transmission lines in the system, determine the energy spent to send a rising step input through them at a time. Hence, determine power dissipation.

e) In a (**0 to 2.5 V**) digital system, swing independent noise is **500mV**, and swing dependent noise fraction **Kn = 0.2**. Determine the noise margins required for proper operation .Assume $NM_H=NM_L=\frac{V_{swing}}{2}$

[10 marks]

(PTO)

Q2. In a CMOS system, consider circuit of Fig. 1a with transmitter Tx, and receiver Rx. Here **Zo= 60 ohms,** designed for matched Thevenin termination with termination voltage Vterm (at V2 node)= **1.25 V**.

Equivalent circuit of **Fig1a** is shown in **Fig. 1b.**

a) Derive the expressions of R1, and R2 in terms **Vdd,** and **Vterm**. Receiver 'Rx' switch point= Vtt= **Vdd/2**. Hence, determine the values required for **R1,** and **R2** resistors.

b) Determine the time of flight through the interconnect if length of interconnect is **6mm**. Take velocity of electromagnetic wave in wire = **1.5 mm/nS**

c) Determine voltage at node **V1** for matched source termination.

d) Re-estimate the voltage at node **V1** if resistance of transmitter 'Tx' is made **15 ohms** only. What will be its draw back/s?

[8 marks]

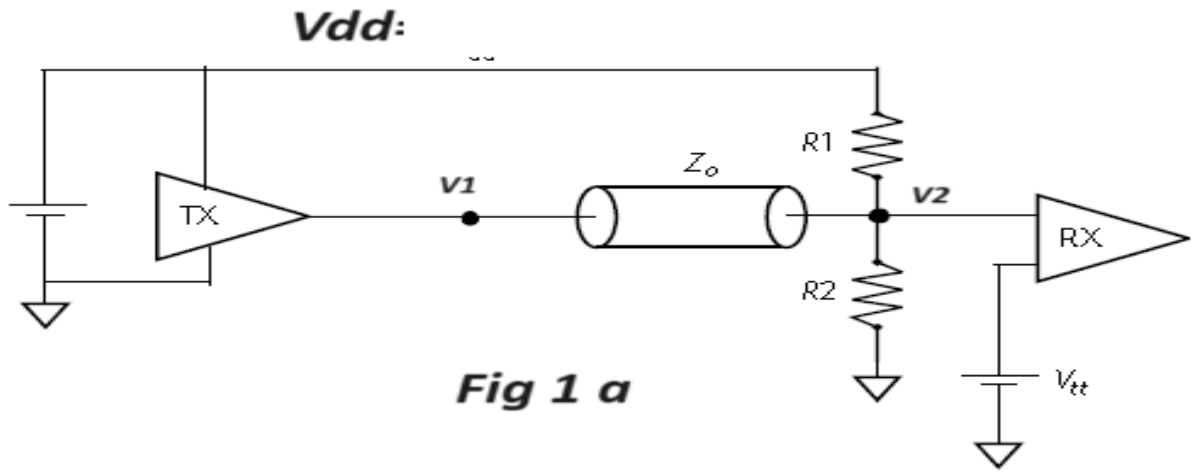

Fig 1 a

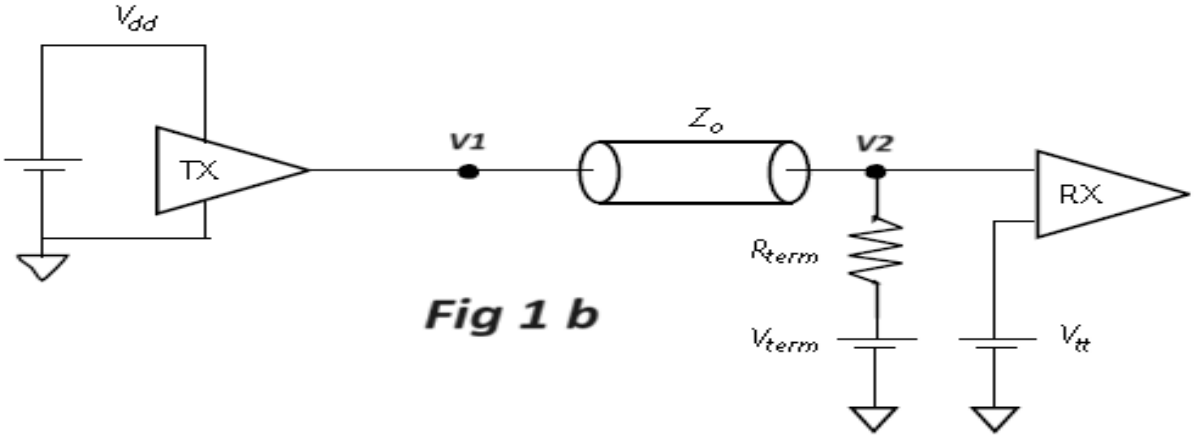

Fig 1 b

(PTO)

Q3. Consider clock distribution circuit of Fig. 2 distributing ***Clk***, and $\overline{Clk}$ signal derived from master clock of frequency **with** 50 % duty cycle and frequency **100M Hz.**

The inverter in buffered clk tree are designed using skewed DCVSL logic ([***Wp/Wn)=1/1***] to generate both ***Clk***, and $\overline{Clk}$ signals simultaneously. Assume that both ***Clk***, and $\overline{Clk}$ signal distribution (at destination) have similar timing noise i.e clock skew of ***±0.1nS***, and no clock jitter .

Assume the skew between ***Clk***, and $\overline{Clk}$ s edges is **0 nS**

Each load destination is a positive edge triggered pipeline with stages operating with *clk*, and $\overline{Clk}$ signal alternatively.

a) Determine the least path delay, $\bar{D}$**,** (insertion delay) of chain of DCVSL inverters in buffered clock tree. Assume **H=100** for calculations. Determine *time-constant of 250nm tech. node*.

b) Also, find new frequency at which pipeline (at destination) can operate taking ***Clk*** / $\overline{Clk}$ skew in consideration. **Take Tseup= Thold= Tc-q=0**

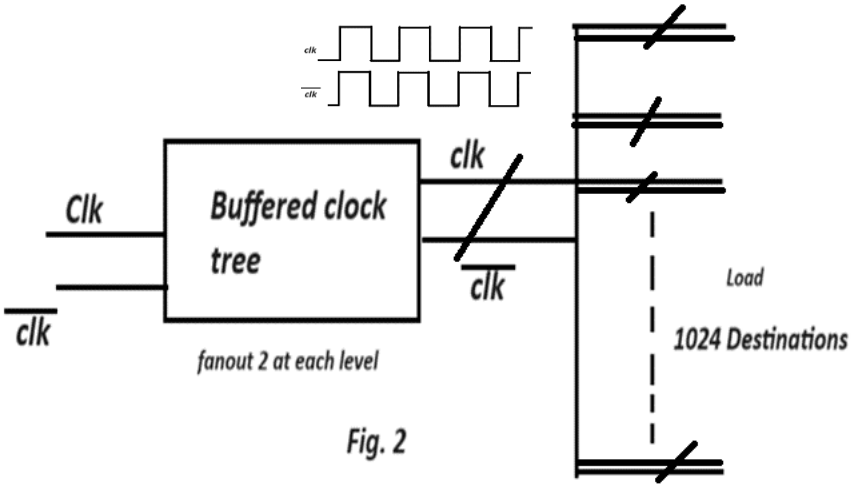

Fig. 2

c) Now in part (b), if additional skew between ***Clk***, and $\overline{Clk}$ s edges is **0.01nS,** re-estimate frequency at which pipeline (at destination) can operate. Take **Tseup= Thold= Tc-q=0**

[8 marks]

Q4. Consider the synchronizer Circuit shown in Fig. 3, using identical D flip flops. T1, T2, T3 are delay elements

- Receiver system clock frequency is 1 M**Hz. Take** flip-flop parameters as —**Tsetup= Thold= Tc-q= 0.1uS,** data signal rise/ fall time = **0.1 µS**
- **A**verage frequency of asynchronous data input is **100 KHz**,
- Time constant of bi-stable element of D-latch=**0.1 µS.**

a) Determine the value of mean time between failure (**MTBF**) for 2 stage D-FF synchronizer shown in encircled box.

b) Re-estimate the value of (**MTBF**) when all parallel synchronizers are operating.

c) For part (a), a Schmitt trigger circuit is inserted at node **O1**. If its low and high thresholds are at voltages midway between ($\mathbf{V_{IL}}$-$\mathbf{V_M}$)**,** and ($\mathbf{V_M}$-$\mathbf{V_{IH}}$) respectively. Given $\mathbf{V_M}$ is midway between $\mathbf{V_{IL}}$**,** and V_{IH}. Re-estimate the value of (**MTBF**)

[5 marks]

(PTO)

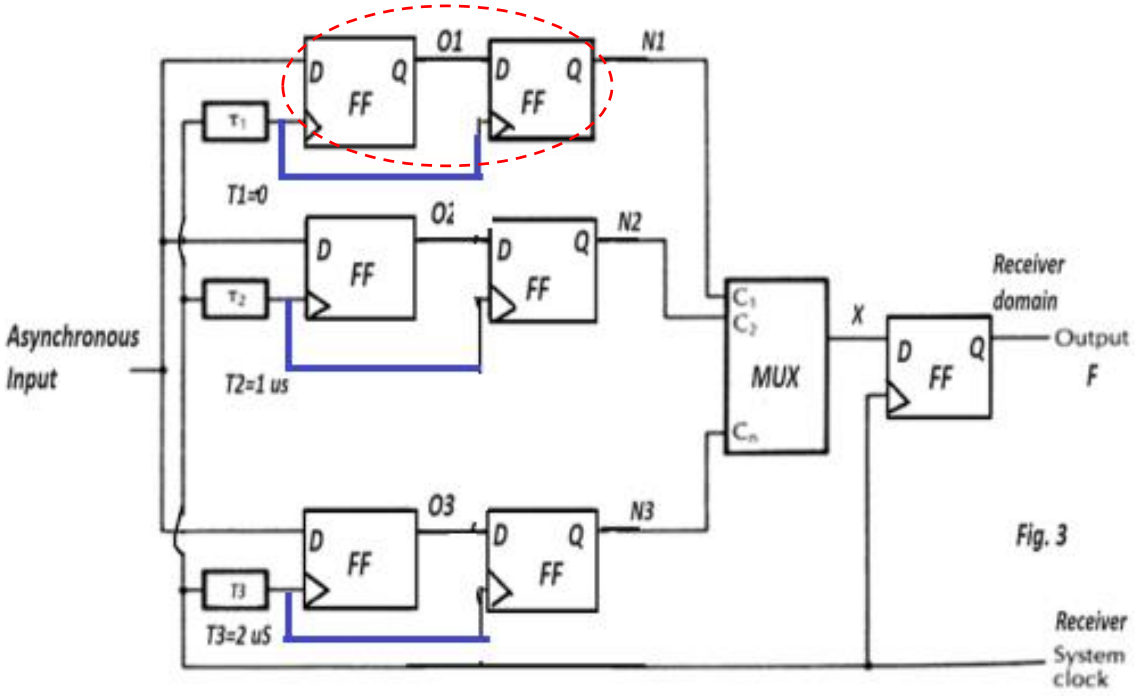

Fig. 3

Q5. Consider the circuit shown in Fig. 4. Φ_E, and Φ_L are two phases of the master clock 'Φ' (wih clock period= **15nS**) in a positive edge triggered synchronous data pipeline. Φ_E phase comes **1 nS** earlier *wrt* Φ clock edge, and Φ_L phase comes **1 nS** late *wrt* Φ clock edge.,

Combinational logic block 'CLB1' has (max/ min) propagation delay T_{pd} and T_{cd} respectively.

D flip flop has parameters $T_{setup}=T_{hold}= T_{clk-q}= 2$ **nS**

For proper operation of pipeline:

a) Determine the constraint on maximum CLB1 delay 'T_{pd}'

b) Determine the constraint on minimum CLB1 delay 'T_{cd}'

[5 marks]

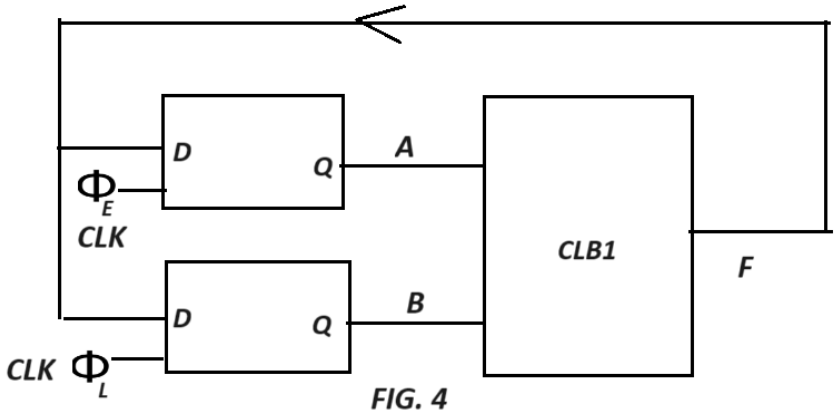

FIG. 4

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