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MIDSEM TEST CLOSED BOOK (9 Oct. 2023) AN2
MEL G623 ADVANCED VLSI DESIGN

TIME-90 MTS. **MAX. MARKS=25**

NOTE: Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat. NO MARKS for unnecessary theoretical explanation. Justify your answers

Vdd=3.3 V, Cox= Fox=0.4 pF/um^2, W_{min}=L_{min}= 1 um

|Vtn|= |Vtp|= 0.7V, , u_nCox= 120 uA/ V^2, u_pCox= 60 uA/ V^2, Rnmos= $\frac{15kohm}{unit\ (W/L)}$.

For standard CMOS inverter, g=1, p=1, tphl= tplh, 1 C_{gmin}= W_{min} L_{min} C_{ox}

Sheet resistance of metal layer of interconnect = 10 ohm

Q1. Consider the clock distribution of Fig. 1, and Fig. 2. Each Spine has clock tree with final 1024 destination points and a fanout of 2 at every level. Take, all inverters/ buffers are identical . Logic blocks connect to spine using "comb" architecture. Assume every inverter/ buffer has 3Cg,min capacitance at its input .

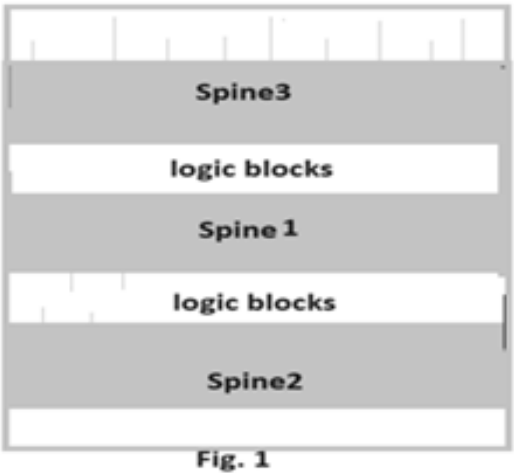

Fig. 1

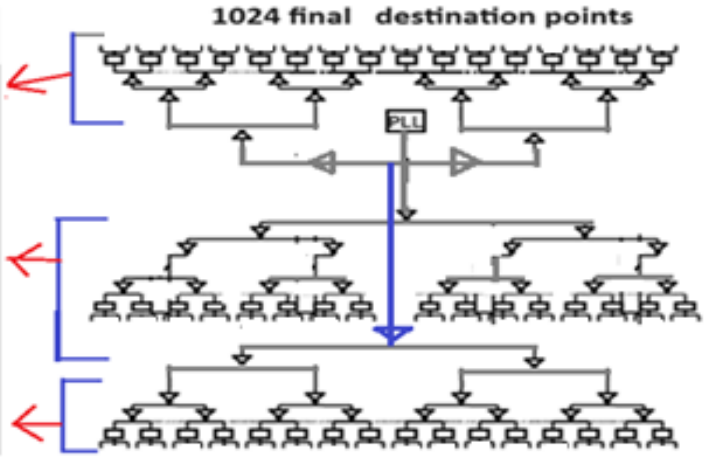

Fig. 2

---Assume length of all wire segments are same in clock tree with wire height/ thickness of 10 um..

---Assume capacitive load at final destination is identical to intermediate level load.

---Assume max tolerable skew is ±100 pico sec.

---Given the total length of wire from source to destination is 1mm

a) Determine wire segment width for ± 15 % process variation .Also find buffer delay.

b) Calculate Resistance of entire wire length (R_W), and capacitance (C_W) of entire wire length.

c) Determine the maximum number of levels (or depth) in clock tree in each spine.

d) Determine the optimum number of buffers (N) to be inserted along the entire length of wire for each spine.

e) Hence find the insertion delay from source to destination path.

[12]

Q2. Answer the following with proper justification

a) Consider Fig. 3. Assuming that a clock skew of +20 ps appears between (FF1, FF2). If Data path is designed using closed loop, global clock timing approach, how will the operating frequency will change. if bit-cell time "Tclk" is 1ns for data path. Assume all buffers identical

b) **Statement**---For Fig. 3., the data path pipeline (open loop, global clock) has less timing uncertainty with decrease in depth of clock tree but more short-circuit power consumption ---. ***YES/NO***. Justify your answer?

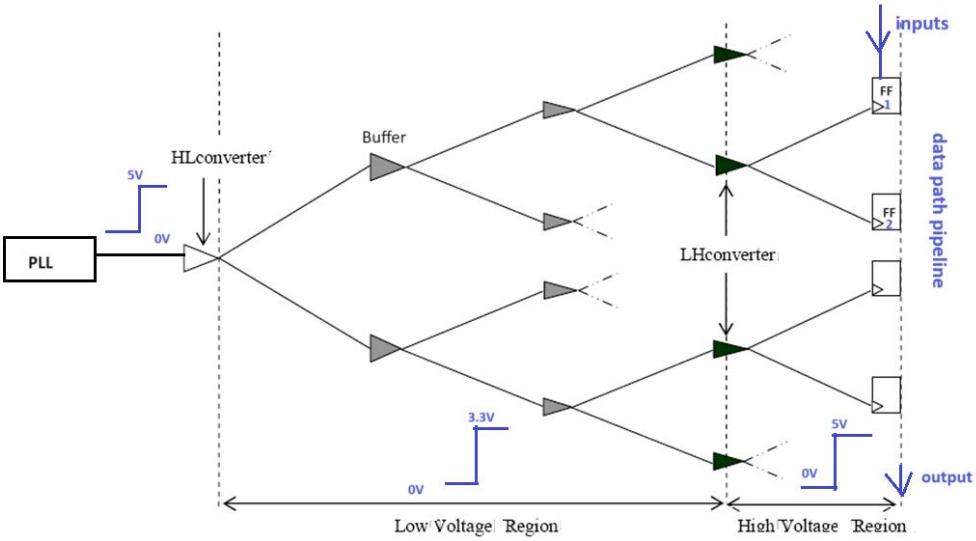

Fig. 3

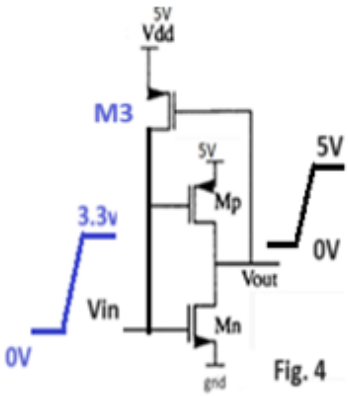

Fig. 4

c) A low Vdd to high Vdd converter is shown in Fig. 4. Justify that it will have zero static power consumption.

d) For fig. 2, what should be the optimum number of buffers 'N' to be inserted for minimum insertion delay using method of logical effort. Assume all buffers identical and best stage effort (ρ) = 3.5. For calculation consider path from source to destination. Ignore segment length delay here.

[10]

Q3. A data path pipeline is designed using 4 phase self-timed approach . The flip flops are replaced by clocked NMOS pass transistor (latch)

Neatly Sketch and label the schematic of 4 stages of self-timed pipeline (push channel). . Assume initial Request signal is available. Minimize power consumption of the schematic.

List the drawback of your implementation.

[5]

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