BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANII SEMESTER 2022-2023
MEL G624 Advanced VLSI Architectures
Mid-Semester Exam: (CLOSED BOOK)
M.M:30 **DURATION: 90 MIN** **10-10-2023**

Q1. Briefly define the three types of cache misses. Assume the baseline cache is set associative. Now, consider the following modifications and analyze the effect of these modifications on each of the types of cache misses(increase, decrease, or no effect). Tabulate your answers in the table given below.

Table. 1

	Name of the :		
	Type of cache miss	Type of cache miss	Type of cache miss
Part a)			
Part b)			
Part c)			
Part d)			
Part e)			

a). If you double the associativity (capacity and line size constant)
b). If you halve the line size (associativity and no of sets constant)
c). If you double the number of sets (capacity and line size constant)
d). Suppose, you are allowed to insert a prefetching unit
e). Suppose you are going to add a buffer **[5M]**

Q2. Consider cache architecture discussed in class.
a). Briefly define way prediction and draw a labelled block diagram of the cache architecture with way prediction unit. Also, explain its benefits/drawbacks and its effect on cache performance?
b). Explain blocking and non-blocking caches with labelled block diagram ? Now, discuss each of them and how does it help in degrading/improving processor's performance? **[5M]**

Q3. Consider a 2-way set associative cache memory with 16 byte lines and a total capacity of 4kB. Assume that the cache has 90% hit rate, and that the way-predictor is right 75% of the time there is a cache hit. Given that a cache hit with a correct way-prediction will take 2 cycles, a cache hit with an incorrect prediction will take 4 cycles, and a cache miss (way-prediction irrelevant) will take 60 cycles to supply data to the processor.

a). Compute the average memory access time (AMAT) of the cache with way-prediction.
b). Without way-prediction (the original 2-way set associative cache) has the same hit rate and miss time, but a 3 cycle hit time. By how many cycles does way-prediction improve the average memory access time?

[5M]

Q4. The first version of a processor performed floating point arithmetic operations in software. The second version of the processor has floating point hardware incorporated in the execution unit, which gives a speedup of 2**0** for the floating point operations over the first version. Simultaneously, it also gives a factor of **4** improvement in energy consumption per floating point operation. What will be the overall improvement in

a). Performance

b). average power consumption

for a program in which in the first version of the processor **50%** time consumption and **50%** energy consumption was due to floating point arithmetic operations? **[5M]**

Q5. Suppose your team have designed a system with the page sizes of 8192B, virtual address space of 64-bit and 48-bit physical address space. The system uses cache of 32KiB, 4-way set-associative as L1 cache with 64B block size. The system also requries an L2 cache with 256KiB, 4-way set-associative L2 cache with 64B block size. Assume TLB entries contain 8 bits of metadata. **[5M]**

Now, for the above system answer the following:

a). Calculate no of bits for Physical page number

b). No of bit for Virtual page number

c). No of bits for Page offset

d). No of bits for Cache block offset

e). No of bits for L1 cache tag

f). No of bits for L1 cache index

g). Size of L2 cache tag(in bits)

h). Size of L2 cache index(in bits)

Q6. With reference to VMIPS architecture mark the following statements as right(√) or Wrong(X) or give a brief answer where ever applicable.

a). VMIPS vector operand elements can be 16/32/64 bit size.

b). VMIPS vector instructions do not permit any scalar operand

c). VMIPS has no branch instruction

d). VMIPS can selectively operate on some elements of a vector and not others

e). VMIPS permits the programer to use a variable vector size.

f). For the same function in comparision to a MIPS program a VMIPS program

- reduces instruction fetches
- increases data fetches

g). What is the total bit-storage capacity of all the vector registers in VMIPS

h). What are the number of input ports and output ports in VMIPS register file.

i). Given a memory latency of 15 clock cycles, how many clock cycles will VMIPS load/store unit take to load/store a vector of size 40 ?

j). There can only be structural hazards but no data hazards in a VMIPS program. **[5M]**

************************************VMIPS Vector Instructions:************************************