Advanced Analog & Mixed Signal Design (MEL G 625)

Date: 18-12-2022 Time: 10:00 hours to 13:00 hours

Duration: 180 minutes Closed Book Full-Marks: 40

Attempt All Questions. Please use the Table given at the end to select appropriate values wherever they are not given in the question.

1. **For the switch given in Fig. 1, derive the expression of V_{out} (in V) versus time (t) and if V_{clk} = V_{in} = 3V and estimate V_{out} (in V) at t =1 ns. Estimate the time (in ns) at which V_{out} is within 10% error from its final value. Ignore channel length modulation and body effect, assume intially the charge on C_H = 0.**
   For a non-inverting SC amplifier if C_1 = $10C_2$ = 10pf and C_{in} = 0.1 pf, calculate the gain error (in%) for the OL gain of 1000.

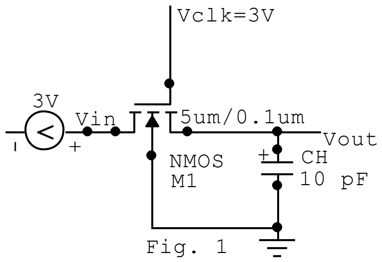

Fig. 1

2+2+4+2 = 10-marks

2. **A type-1 PLL has ω_{LPF} = 1 Mhz, K_{VCO} = 100 Mhz/ V and K_{PD} = 1 V/ rad. Derive the transfer function, estimate the poles and determine the step response of the PLL if a frequecy step of $\Delta\omega_{in}$ is given at time t = t_1 on ω_{in}. All frequencies and phases must be in rad/s and rad. Draw a plot (need not be to scale) indicating different parameters at required places.**

4+4+4+2 = 14-marks

3. **Sketch a double balanced Gilbert Quad Mixer and denote drain current expressions with appropriate subscripts for *i.f.* as applicable. Show the terminals for inserting V_{lo} and V_{rf}. *No description of operation is needed*.**

   If the aspect ratios of all he MOS devices are 50.0μm/0.5μm and V_{rf} = 2V for, estimate the load resistance such that the conversion gain is 20dB.

(2+2+1+1)+2 = 8-marks

4. **For a 2-amplifier latch, derive the time taken (T) to reach the required value (V_{XY1}) that can be accepted as a valid login level, starting from initial value of V_{XY0}, provided that the open look gain of the amplifier is $-A_0$ and the time constant is τ_0.**
   If the sampled value has a uniform distribution between $\pm$ V_{XY1} then estimate the probability of metastability in a comparator latch if A_0 = 1000, τ_0 = 100 ns and the circuit operates on a 2Ghz clock.
   For an 8-bit ADC, what should be maximum clock-jitter duration in order to keep the sinusoidal analog input (of 50mV peak to peak value and 1Mhz frequency) to vary by less that 1-LSB?
   Which of the two potential errors are suppressed by Gray encoding in flash converters?

2+2+2+2 = 8-marks

[i]**Table of Values**

Parameters	V_{Th}(V)	γ ($\sqrt{V}$)	ϕ_f(V)	L_D (m)	λ(V^{-1}) for L_{Geo}=0.5μm	$\mu_{n/p}C_{OX}$(A/V^2)
NMOS	0.7	0.5	0.9	0.08×10^{-6}	0.1	134.26×10^{-6}
PMOS	-0.8	0.4	0.8	0.09×10^{-6}	0.2	38.36×10^{-6}
Common	$n_i = 1.45 \times 10^{10} cm^{-3}$, q= 1.6× $10^{-19}C$; k = 1.38× $10^{-23}\frac{J}{K}$; V_{DD}= V_{Ck}= 3.0V; V_{SS}= 0 V; β_{NPN}=150, β_{PNP}=100, Room Temperature= 27^0C; ε_{Si}=11.68; ε_{SiO_2}=3.6; ε_0= 8.85 × $10^{-12}\frac{F}{m}$; $C_{GDO_{NMOS}} = 0.4 \times 10^{-9}\frac{F}{m}$; C_{ox}=6.9 $fF/\mu m^2$ for t_{ox}= $50\dot{A}$					

Table of Equations (*You might have seen in a distant galaxy....*)

1.	$I_D = \frac{1}{2}\mu_{n/p}C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$; $I_D = \frac{1}{2}\mu_{n/p}C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$ when channel length is included
2.	$\phi_0 = \frac{kT}{q} ln\left(\frac{N_D N_A}{{n_i}^2}\right)$
3.	$Q_{B0} = -\left(1 - \frac{\Delta L_S + \Delta L_D}{2L}\right)\sqrt{2q\epsilon_{Si}N_A\|2\Phi_F\|}$
4.	$C_{j0} = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_D N_A}{N_D + N_A}\right)\frac{1}{\Phi_0}}$
5.	$\Delta V_{T0} = \frac{1}{C_{ox}}\sqrt{2q\xi_{Si}N_A\|2\Phi_F\|}\cdot\frac{x_j}{2L}\cdot\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right]$
6.	$x_d = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_D N_A}{N_D + N_A}\right)(\Phi_0 - V)}$