Advanced Analog & Mixed Signal Design (MEL G 625)

Date: 31-10-2022 Time: 09:00 hours to 10:30 hours Duration: 90 minutes

Closed Book Full-Marks: 20

Attempt All Questions. Please use the [i]Table given at the end to select appropriate values wherever they are not given in the question.

1. **For Fig. 1(a) below derive from first principle the normalised expression of non-linearity in voltage-gain. Calculate the nonlinearity (%) if V_{id} = 50.0 mV. For Fig. 1(b), assuming $\xi >> \xi_C$, estimate the voltage gain provided that saturation velocities of NMOS and PMOS are in the ratio of μ_n/μ_p. Device dimensions in μm are indicated as applicable.**

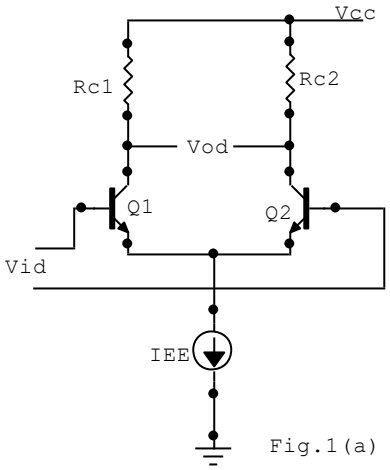

Fig.1(a)

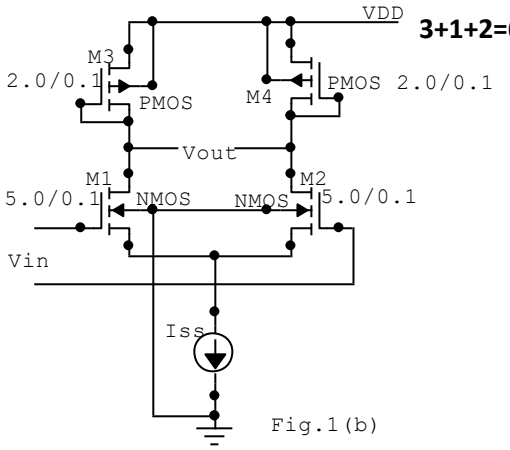

Fig.1(b)

3+1+2=6-marks

2. **A clock of 50% duty cycle at $\bar{\phi}$, operates a latch comprising of 2-back-to-back amplifiers of identical gain 100 and a characteristic time constant 16 μs. If the output-difference needs to be 0.2 V to be interpreted as a valid logic, what is the peak clock-frequency at which the output logic-level can be correctly interpreted if the worst case input difference is 2 mV.**

What resistance does the SCP see looking into the drain of M7 in circuit of Fig. 2 to maintains a CMFN? What shall be the mode of operation of M5(6) for this?

3+2+1= 6-marks

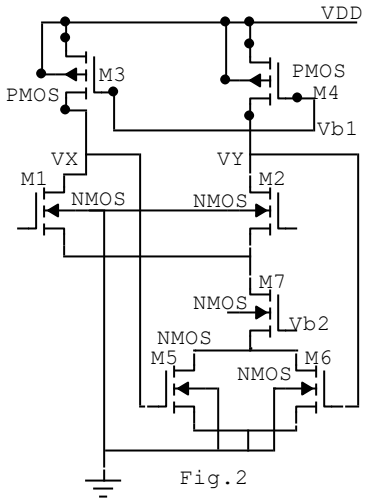

Fig.2

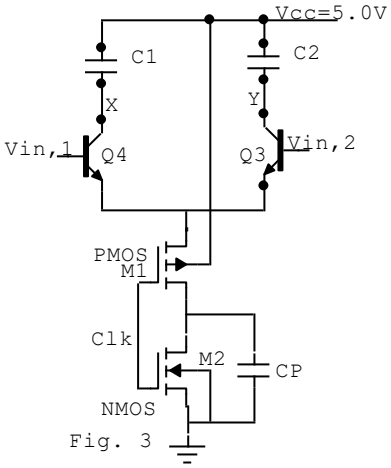

Fig. 3

3. **the equivalent circuit of Fig 3, assuming the input CM-level ≈ V_{CC}, V_{BE} and $R_{on\text{-}M1}$ to be constant. Estimate the small signal voltage gain at t = ∞, if V_{BE} = 0.7V, $2C_p=C_1=C_2$=10 pf.**

2+2= 4-marks

4. **Which variation of 2-step ADC architecture makes the subtractor redundant? With a neat sketch briefly describe its operation for a-10-bit configuration with each step resolving for 5-bits.**

1+3= 4-marks

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[i] **Table of Values**

Parameters	V_{Th}(V)	γ ($\sqrt{V}$)	ϕ_f(V)	L_D (m)	λ(V^{-1}) for L_{Geo}=0.5µm	$\mu_{n/p}C_{OX}$(A/V^2)
NMOS	0.7	0.5	0.9	0.08×10^{-6}	0.1	134.26×10^{-6}
PMOS	-0.8	0.4	0.8	0.09×10^{-6}	0.2	38.36×10^{-6}
Common	$n_i = 1.45 \times 10^{10} cm^{-3}$, q= $1.6\times 10^{-19} C$; k = $1.38\times 10^{-23} \frac{J}{K}$; V_{DD}= V_{Ck}= $3.0V$; V_{SS}= 0 V; β_{NPN}=150, β_{PNP}=100, Room Temperature= $27^0 C$; ε_{Si}=11.68; ε_{SiO_2}=3.6; ε_0= $8.85 \times 10^{-12} \frac{F}{m}$; $C_{GDO_{NMOS}} = 0.4 \times 10^{-9} \frac{F}{m}$; C_{ox}=6.9 $fF/\mu m^2$ for t_{ox}= $50\dot{A}$					

Table of Equations (*You might have seen in a distant galaxy....)*

1.	$I_D = \frac{1}{2}\mu_{n/p}C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$; $I_D = \frac{1}{2}\mu_{n/p}C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS})$ when channel length is included
2.	$\phi_0 = \frac{kT}{q} ln\left(\frac{N_D N_A}{{n_i}^2}\right)$
3.	$Q_{B0} = -\left(1-\frac{\Delta L_S + \Delta L_D}{2L}\right)\sqrt{2q\epsilon_{Si}N_A\lvert 2\Phi_F\rvert}$
4.	$C_{j0} = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_D N_A}{N_D+N_A}\right)\frac{1}{\Phi_0}}$
5.	$\Delta V_{T0} = \frac{1}{C_{ox}}\sqrt{2q\xi_{Si}N_A\lvert 2\Phi_F\rvert}.\frac{x_j}{2L}.\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right]$
6.	$x_d = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_D N_A}{N_D+N_A}\right)(\Phi_0 - V)}$