**Birla Institute of Technology & Science**

I[st] Semester 2016-17

MEL G626 VLSI Test and Testability

Comprehensive Examination (Closed Book)

**MM:35** **Time: 3 Hrs** **Date: 07/12/2016 (AN)**

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***Instructions: Attempt at parts of a question together***

**Q1: (i)**

**(A)**Write the result displayed after running the following system verilog program.

```
module abc();
initial
begin
int d [], xyz[], j;
int tq[$], x[$];

d=new[5];
foreach (d[j])
 d [j]= 100*j;
xyz=d;
foreach (xyz[j])
 xyz [j]= d [j]*2;
$display ("%p",d);
$display ("%p",xyz);
d=new[10] (d);
tq=d;
$display ("%p",tq);
tq.insert(2,3);
$display ("%p",tq);
tq.delete(5);
$display ("%p",tq);
tq.push_front(7);
$display ("%p",tq);
j=tq.pop_back;
$display ("%d",j);
x=tq.unique();
$display ("%p",x);
end
endmodule
```

**(3)M**

**(B)** Write if any error in the following system verilog program else write its output after running the code.

```
class A ;
int j;
static task incr();
j=j+1;
$display("j is %d",j);
endtask
endclass
```

```
program main ;
A obj_1;
A obj_2;
initial
begin
obj_1 = new();
obj_2 = new();
obj_1.incr();
obj_2.incr();
end
endprogram
```

**(2)M**

**(ii)** Write the three basic operations for a semaphore? **(1)M**

**(iii)** List the several 'structural coverage models' used for simulation based verification. **(1)M**

**(iv)** Write the types of 'Golden Vector Testbench'. **(1)M**

**Q2:** For the circuit shown in Fig 1, (i) mark all faults (ii) remove faults using fault equivalent collapsing and compute the collapse ratio. (iii) remove faults using fault dominance collapsing (including fault equivalent collapsing) and compute the collapse ratio. **(3) M**

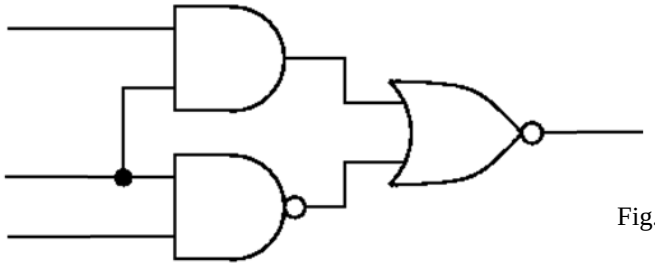


Fig. 1

**Q3:** For the circuit shown in Fig. 2, explain if the test vector a=1, b=1 using the parallel fault simulation can detect the faults S-a-0 at 'c' and S-a-1 at 'f'. Write the minimum size of vector required and indicate all the steps. **(2)M**

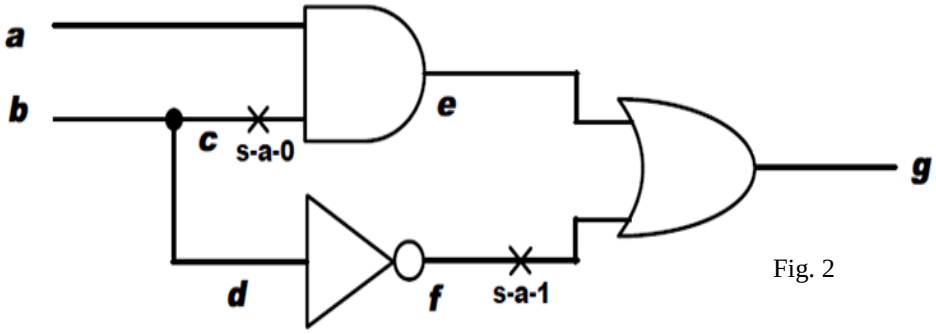



Fig. 2

**Q4:** For the circuit shown in Fig. 3 use the 'fault table computing' method to find all the test vectors required to test the circuit. Show all the steps. **(3)M**

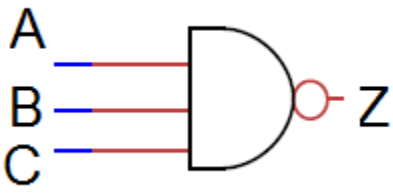



Fig. 3

**Q5: (A)**
For the circuit shown in Fig. 4, use D-algorithm to detect SA0 fault at node 'a' ? Use implication procedure using primitive D-cube of failure (PDFC), propagation D-cubes (PDC), singular cover (SC), D-intersection to show values at each note in every steps. **(3)M**

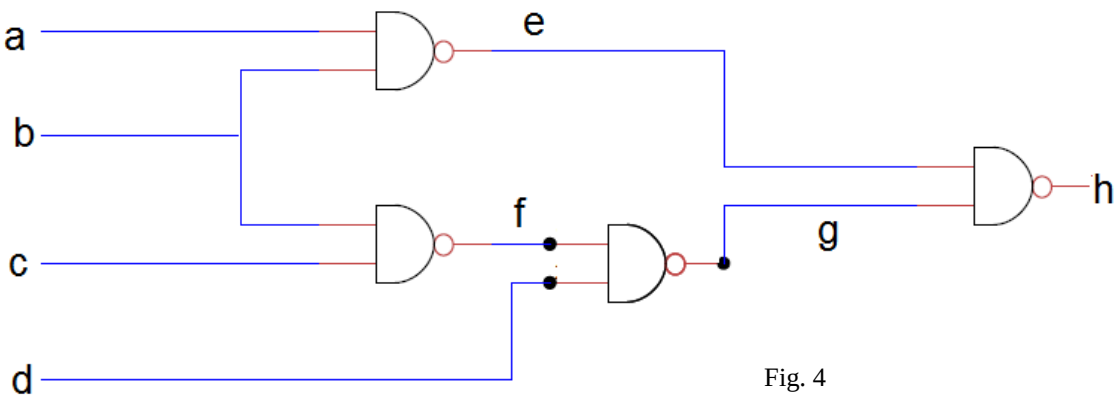



Fig. 4

**Q5: (B)** For the circuit shown in Fig.5 apply PODEM to detect stuck at 1 fault at node g, show all the steps. **(2)M**

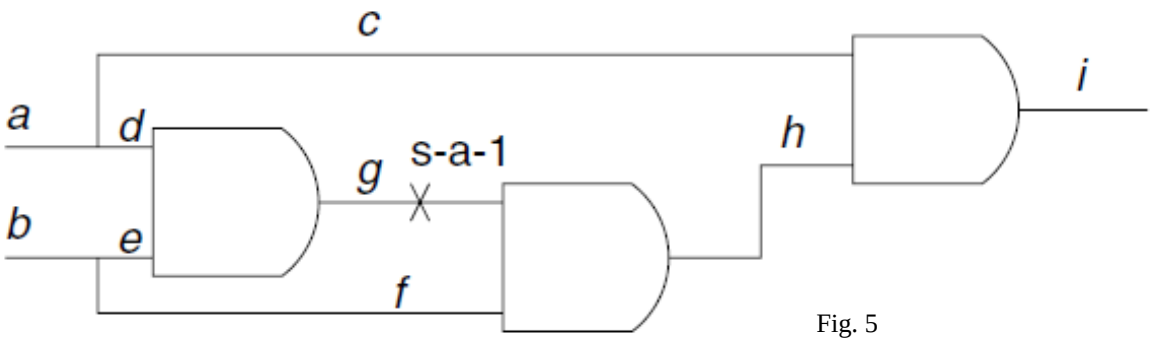



Fig. 5

**Q6:** For the circuit shown in Fig.6, compute SCOAP combinational controllability and observability measures for all lines. Assuming that the testability of a stuck-at fault can be represented as the sum of appropriate controllability and observability, find the set of most difficult to test fault. **(4)M**

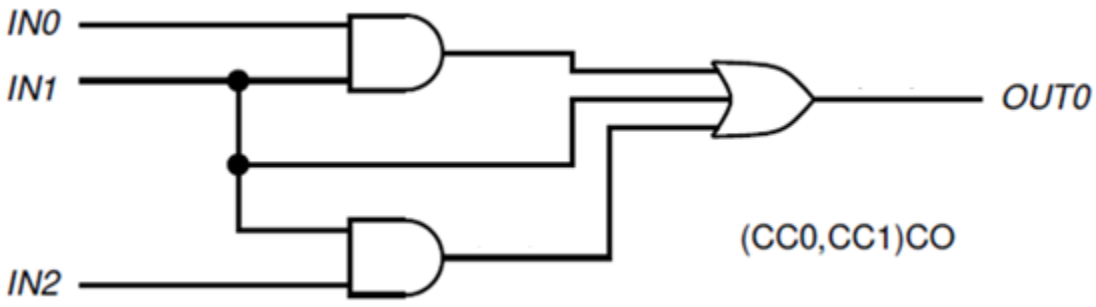



Fig. 6

**Q7:**

**(A)** Determine the test sequence for the stuck at One (SA1) fault on the indicated line of the circuit as shown in Fig 7. **(3)M**

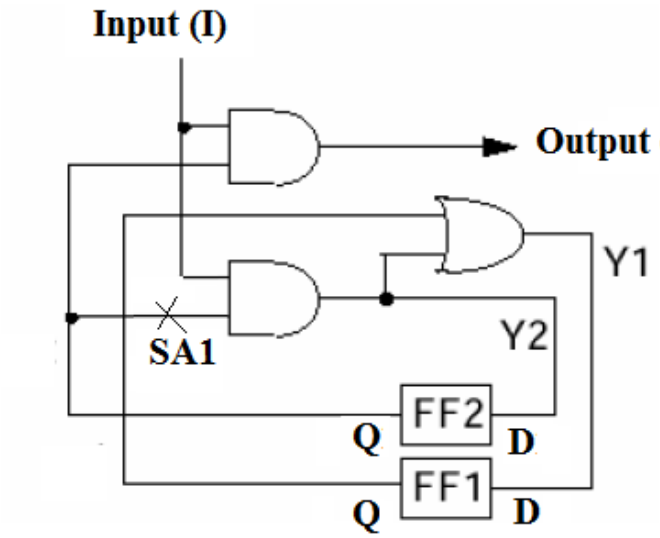
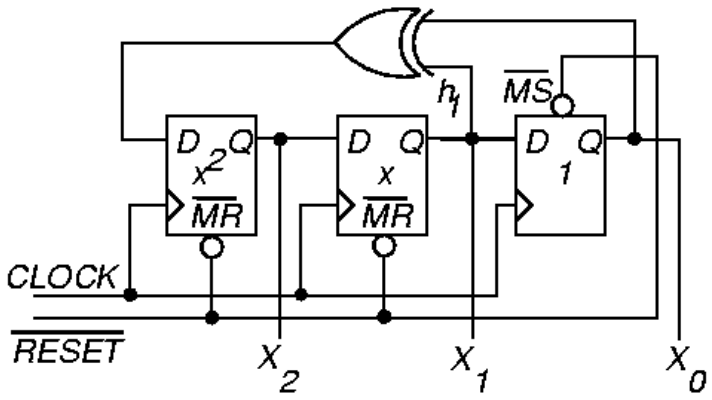



Fig. 7

**(B)** A scan chain having number of scan flops 20 is used to test 10 combinational vector. Calculate the number of clock periods required to complete the test if (assume scan registers are already tested). **(2M)**

**Q8:**

**(A)** Write the companion matrix for the following LFSR circuit. **(2M)**




**(B)** Describe Indempotent coupling fault with proper state diagram and name a Test which can detect this fault. What is the complexity of the algorithm in terms of *n*? **(3 M)**

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