Birla Institute of Technology & Science
Ist Semester 2016-17
MEL G626 VLSI Test and Testability
Test-1 (Closed Book)

MM:20 **Duration: 50 Min** **Date: 27/09/2016**

Q1:

(i) Why is it not possible to verify functionality of a chip exhaustively? Explain with suitable example. **(1M)**

(ii) Explain the meaning of defect level 237,700 ppm. **(1M)**

(iii) What are the non-HDL assertions? Describe its types. **(1M)**

(iv) Explain the functional verification test coverage in brief. **(1M)**

(v) Explain the any two advantages of bootstrapping in the verification process. **(1M)**

(vi) Explain the advantage of using emulation in the verification process. **(1M)**

Q2: What are the possible ways in which stimulus can be generated for simulation based verification. Write an algorithm for stimulus generation at a single port of the Calculator 2. **(3M)**

Q3: For a 'calculator 2' use parameter biasing to pre-generated random test cases for 100 stimuli as per following requirements: (i) legal commands 90% of the time and illegal commands 10% of the time. (ii) Where any legal command such as add, sub, shift left and shift right are equally generated. (iii) For each port these command should be equally generated. (iv) The delay between command should be '0 cycle' for 50% command and '1 cycle' for remaining 50% commands. Write the template file and randomization control parameters. **(3M)**

Q4: What are the differences between a golden vector test bench and cycle accurate reference model test bench verification environment? Describe the merits and demerits of both the self-checking test benches. **(3M)**

Q5: Explain the dynamic mapping mechanism to support vertical naming issues? **(2M)**

Q6: Explain the benefits of separation of HDL domain and test bench domain. Also using a suitable diagram explain the control flow interaction between HDL model and test-bench model in a separated C/C++ test bench. **(3M)**

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