Birla Institute of Technology & Science
Ist Semester 2017-18
MEL G626 VLSI Test and Testability
Comprehensive Examination (Closed Book)

MM: 25 **Time: 1.30 Hrs** **Date: 01/12/2017 (AN)**

Note: Solve all part of a particular question together in sequence.

Q1: Determine the test vectors to detect the (i) Stuck open (ii) Stuck short fault for the NMOS transistor indicated in the Figure 1. Also show faulty and and fault free output. **(2 M)**

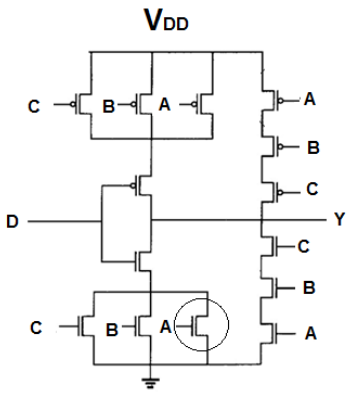

Figure 1

Q2: For the circuit shown in Figure 2, (i) Mark all faults (ii) Remove faults using fault equivalent collapsing and compute the collapse ratio. (iii) Further, remove the faults using fault dominance collapsing (including fault equivalent collapsing) and compute the collapse ratio. **(4 M)**

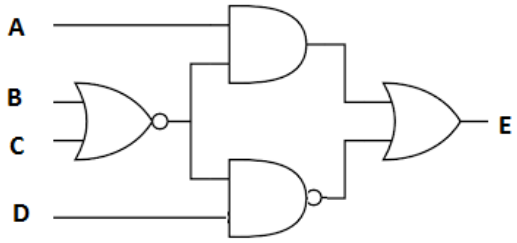

Figure 2

Q3: For the circuit shown in figure 3, use the Boolean difference equation showing all the steps to detect SA0 and SA1 at 'h'. **(3 M)**

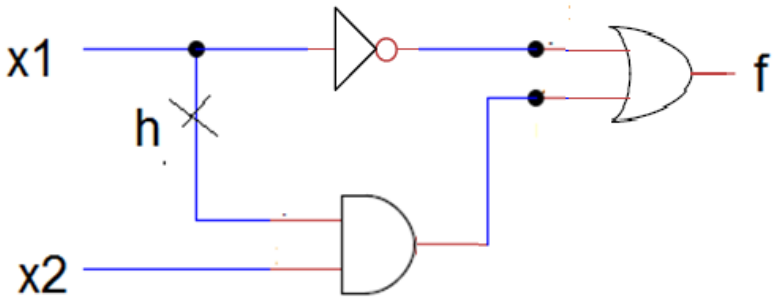

Figure 3

Q4: For the circuit shown in figure 4, use D-algorithm to detect SA1 fault at line '5'? Use implication procedure using the primitive D-cube of failure (PDFC), propagation D-cubes (PDC), singular cover (SC), D-intersection to show values at each note in every steps. **(3 M)**

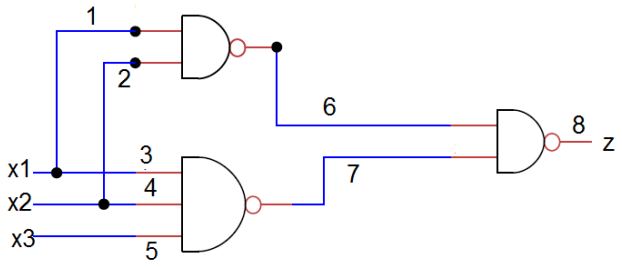

Figure 4

Q5: (i) Calculate the SCOAP controllability and observability measures for a 3-input X-OR gate. **(2 M)**

(ii) For the sequential logic circuit in Figure 5, draw the same sequential circuit with full scan chain design. Discuss its test operation. If number of combinational vectors are 100 then calculate the sequence length? **(3 M)**

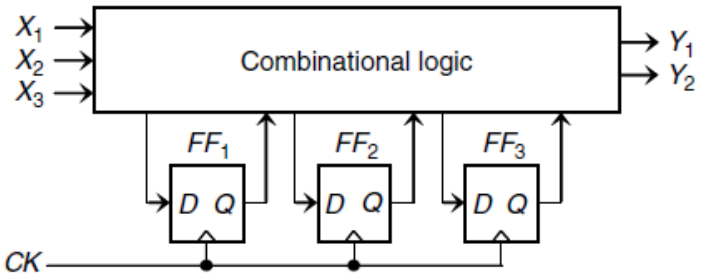

Figure 5

(iii) Explain the difference between PODEM and FAN in terms of backtracking process. **(1 M)**

Q6:

(A) Design a four-stage weighted LFSR with each output having probability of getting a 1 are 0.75, 0.5, 0.25, or 0.125 at its four outputs. **(3 M)**

(B) The MATS+ algorithm : "{ ⇕ (w0); ↑ (r0, w1); ↓ (r1,w0) }"

is applied to a memory with 9 locations as given in the Figure 6. Which kind of fault will this test be able to detect? Draw the output after every step is executed in the algorithm for both fault free and faulty case (if shaded memory location is faulty). **(4 M)**

X	X	X
X	X	X
X	X	X

Figure 6

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