Birla Institute of Technology & Science
Ist Semester 2017-18
MEL G626 VLSI Test and Testability
Comprehensive Examination (Open Book)

MM: 25 **Time: 1 Hr 30 Min** **Date: 01/12/2017 (AN)**

Note: Solve all part of a particular question together in sequence.

Q1 :

(A) A 'calculator 2' uses the parameter biasing to bias pre-generated random test cases for 1000 stimuli as per following requirements: (i) legal commands 85% of the time and illegal commands 15% of the time. (ii) Where legal commands such as add, sub are generated 60% (equally generated) of time and shift left, shift right are generated 40 % of time (equally generated). (iii) For each port these command should be equally generated. (iv) The delay between command should be '0 cycle' for 30% command, '1 cycle' for remaining 40% commands, '2 cycle' for remaining 30% commands. Write the template file and randomization control parameters. **(4 M)**

(B) Explain the drawback of debugging on-the-fly generated test cases? **(2 M)**

(C) Explain how the early functional verification can be performed much before RTL? What are its advantages? **(2 M)**

Q2:

(A) Write the output after running the following system verilog program. **(2 M)**

```
class xyz ;
int i;
int j;
task lmn(i,j);
$display( "i=%d,j=%d", i,j);
endtask
endclass
program main;
initial
begin
xyz obj_1;  xyz obj_2;  obj_1 = new();  obj_2 = new();  obj_1.lmn(10,100); obj_2.lmn(20,200);
end
```

(B) A system verilog task 'incr' is defined inside a class 'A'. Write a single system verilog program such that: (i) it describes two handle of this class as obj_1, obj_2. (ii) it creates object of same class using these handles. (iii) it further, uses these object alternately to calls the same task 'incr' to obtain final print as " J is 1, J is 2, J is 3, J is 4, J is 5. Write the system verilog class 'A' having task 'incr' inside same class such that the required final result are obtained. **(5 M)**

Q3: Generate a minimum set of test vectors (x_1, ……x_n) to detect all single stuck-at faults for a cascade of (n−1) exclusive-OR gates for an n-bit parity checker, as shown in figure 1, where each exclusive-OR gate is implemented by elementary logic gates (AND, OR, NAND, NOR, NOT). **(4 M)**

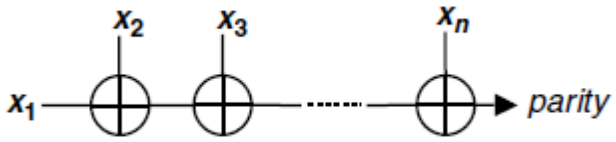

Figure1

Q4: The circuit shown in figure 2, shows rise and fall delays of the different NAND gates (where: a/b represents the rise/fall delay of gate in ps). Find the test vector ABCDE to detect path delay fault for path A-G-J-K if tested for slow to rise. Find the expected delay of path. **(3 M)**

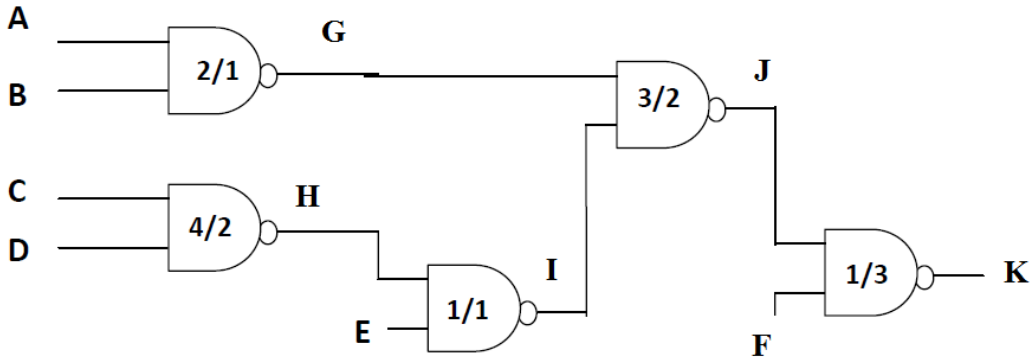

Figure 2

Q5: Suggest the best order for the following function and also draw it's OBDD. **(3 M)**

$f = a_1b_1 + a_2b_2 + a_3b_3$

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