Birla Institute of Technology & Science, Pilani (Pilani Campus)

Ist Semester 2023-24

MEL G626 VLSI Test and Testability (Closed Book)

Mid Semester Examination

Max Marks: 35 Duration: 1.30 Hrs Date: 11/10/2023 (AN2)

Note: ***Attempt all parts of particular question at one place (in sequence).***

Q1: (A) Draw UVM test bench environment and write its different components. UVM is based on which language/s? Also explain the role of transactor. **(3 M)**

(B) What can be an assertion for Calc2 design related to the legal stimulus? **(2 M)**

Q2: For the 'calculator 2' considering that all the commands would be successfully completed, draw the timing diagram for the calculator if only port 2 is loaded with two ADD command followed by a SHIFT LEFT and then a SUB command. Label two operand as OP1 and OP2 in each case and producing good responses and results as R1, R2, R3 and R4 and tags are '00', '01', '10' and '11' respectively. **(3 M)**

Q3: (A) Describe the 'functional verification coverage' method in calculator-2? How we obtain these coverage? Are these task automated? **(4 M)**

(B) Write the sequence of states of stimulus generator for calculator-2 if the command sequences are:
(i) Invalid command, (ii) valid add command (iii) valid add command (iv) valid shift command **(2 M)**

(C) Generate the commands corresponding to following template identify generation type and template type?

Port2: SUB UNDERFLOW Delay 2

Port3: SHL GOODRESP Delay 1

Port4: Illegal Illegal Resp **(4 M)**

(D) What are different self-checking test benches also compare timing checks amongst it. Also Explain the debugging of 'on the fly' test cases? **(4 M)**

Q4: (A) Write the output of following system Verilog Program? **(4 M)**

```
module ABC;
initial begin  bit [8:0] assoc [int], idx=1;
repeat (8) begin assoc [idx] = idx*10;
idx = idx+3; end
foreach (assoc[i])  $display ( "assoc [%h]=%h",i,assoc[i]);
end endmodule
```

(B) Write and explain if any error in the following system Verilog program otherwise correct error and write the expected result displayed after running it . **(4 M)**

```
program xyz1 ();
int a,b;
initial begin
a=5; b=5;
#10 a=15; #10 b=10; #10 a = 15;
#10 b=20; #10 a = 15; #10 a = 25;
#10 b=30; #10 $finish; end
```

```
task  pqr (ref int i, ref int j);
forever   @(i or j)
begin
int mul;   mul=i*j;  $display("a is %0d, b is %0d, mul_is %0d",i,j,mul);
end endtask
initial pqr (a,b);
endprogram
```

(C) The full Adder test bench module (FA_TB) which applies each of input combination of a, b, cin (000 to 111) after every 3 ns and also monitors the applied input along with its corresponding output result. Write a system Verilog program FA_TB and data-flow Full Adder module (FA_DF) which are sharing a common interface (a, b, cin, sum, cout). Write the interface FA_abc using logic data type and instantiate it with name 'p' in both FA_DF and FA_TB module. Also write the top module which is binding this interface and these two modules. **(5 M)**

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