Birla Institute of Technology & Science
I st Semester 2023-2024
MEL G626 VLSI Test and Testability
Comprehensive Examination (Closed Book)

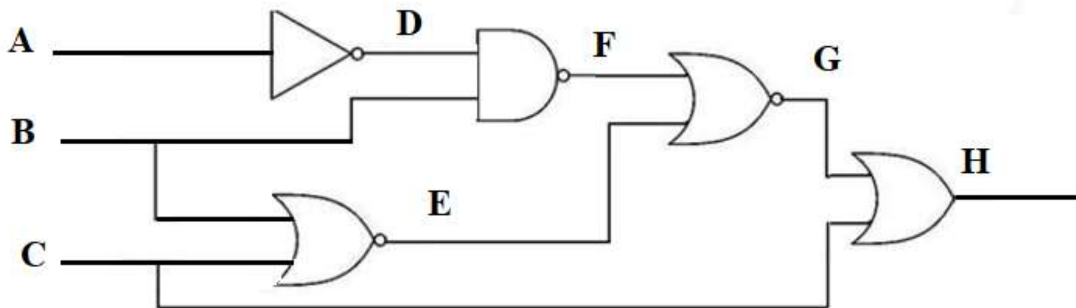
MM: 20 **Duration: 1 Hr. 30 Min** **Date: 12/12/2023**

Note: ***Attempt all parts of particular question at one place (in sequence). Encircle final answer.***

Q1: For the circuit shown in Figure 1, find the following answer by indicating your answer for each step on the separately redrawn figure:

(a) Find the number of all potential fault sites and mark all faults.
(b) Derive the equivalence collapsed set keeping faults towards top and primary inputs. What is the collapse ratio?
(c) Derive the dominance collapsed set. What is the collapse ratio?
(d) Also find the collapse ratio using the check point theorem?
(e) Find the test vector to detect SA0 at F (Note: while assigning 'X' at any gate input prefer the bottom-most input)
(f) Find the test vector to detect SA0 at E and F (Note: while assigning 'X' at any gate input prefer the bottom-most input)
(g) Find the test vector to detect SA1 at B (Note: while assigning 'X' at any gate input prefer the bottom-most input)
(h) If ABC=101 then find thefaults that can be tested using deductive fault simulation (label braching node as 1, 2, 3…. from top to bottom, e.g. for node B branching nodes are B1 and B2). Show fault list at each node.
(i) Find the set of initial and final vector to detect robust 'slow to rise path delay' for path A-D-F-G-H.

[1+2+2+1+1+1+1+3+2=14 M]



Q2: Write the error if any in the following System Verilog program. Also write the output of program? **[3 M]**

```
class Transaction;
function void display1();
$display("Transaction display");
endfunction
endclass
```

```
class PCI_Tran;
Transaction t;
function new();
t=new();
endfunction
function void display2();
$display("PCI_Tran display");
t.display1();
endfunction
endclass
```

```
program xyz ;
PCI_Tran pc;
initial
begin
pc = new();
pc.t.display1();
pc = new();
pc.display2();
end
endprogram
```

Q3: Discuss the row and column addressing bits for a **64*64** memory array. If the word size is 4 then explain the mutual comparator used in the memory BIST? **[3 M]**

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Q1: For the circuit shown in Fig 1:

(i) Compute SCOAP combinational controllability and observability measures for all lines by indicate answers on the redrawn figure.

(ii) Also find the set of most difficult to test fault. **[4+1 M]**

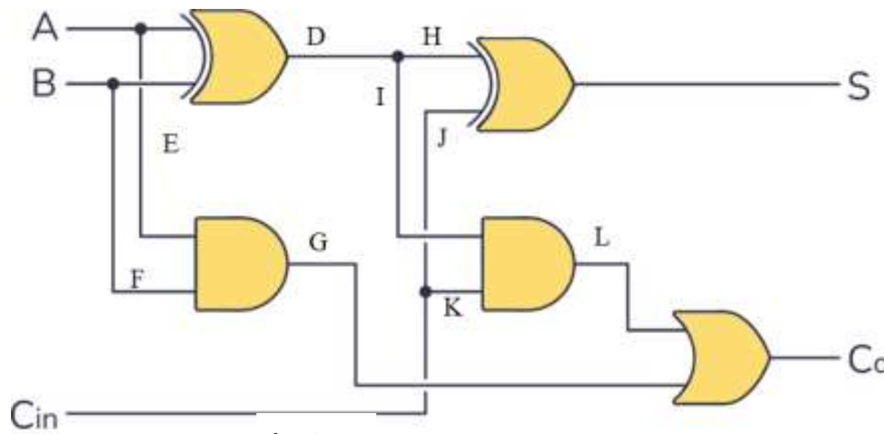

Fig. 1

Q2: Expand the circuit shown in Fig. 2, in to the 3-time frames. Also mark all the signal values using 5 valued Roth's algebra in each time frame to generate a test vector to detect the SA1 fault at 'f'. **[5 M]**

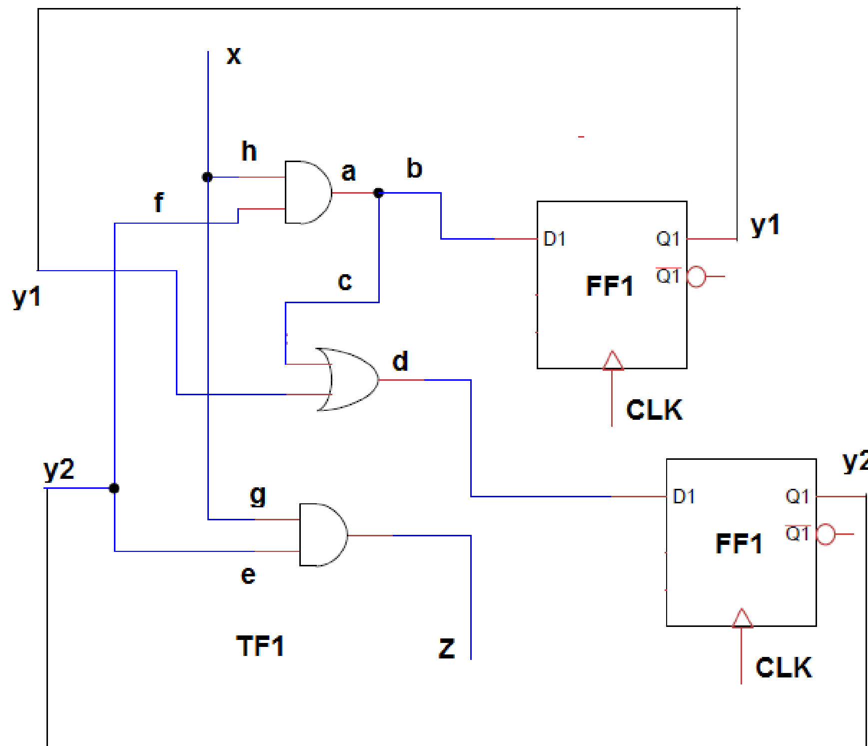

Fig. 2

Q3:

(A) Calculate the % defect level (DL) in ppm if the fault coverage (FC) is 95 % and process yield is 90% ? **[2 M]**

(B) Draw diagram for the compression scan mode and serial mode and explain purpose of it? **[3 M]**

(C) In an enhanced-scan test 100 delay vector pairs are applied where application of each V1/V2 vector require 10 clock cycles, then find the total number of clock cycles required to complete the test.
(Assumption: During scan out of final result output states, scan in of new vector can also be performed simultaneously.) [**3 M]**

(D) For the BIST structure, consisting of LFSR register and MISR find the test time to compress 100 million BIST vectors running at 200 MHz frequency. **[2 M]**

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