BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

COMPREHENSIVE EXAMINATION
Semester I: 2022-2023
Part A: Closed Book
MEL G631: Physics and Modelling of Microelectronic Devices

Date: **27/12/2022** Maximum Marks: **35** Maximum Time: **75 minutes**

Given (Use, if not specified in the questions):
$q=1.6\times10^{-19}$ C, $k=1.38\times10^{-23}$ m^{2}kgs^{-2}k^{-1}, T=300 K, kT/q=0.026 V, $\varepsilon_0=8.85\times10^{-14}$ F/cm
Si: $\varepsilon_r=11.8$, $n_i=1.45\times10^{10}$ cm^{-3}, $E_g=1.12$ eV, $\mu_n=1300$ cm^2/V-s, μ_p(Si)=480 cm^2/V-s, $q\chi=4.05$ eV,
$N_C=2.8\times10^{19}$ cm^{-3}, $N_V=1.04\times10^{19}$ cm^{-3}.
Au: $\varphi_M = 4.75$ eV

Answer should be very brief and to the point.

Q1. Where is the probability of finding of an electron is exactly half (½)? [1]

Ans:

Q2. Suppose, the probability of occupancy by an electron in conduction band is represented by $f_D(E)$. How can we represent the probability of occupancy by a hole in valance band? [1]

Ans:

Q3. If, $E_C - E_F \gg kT$, write the Fermi function using Maxwell-Boltzmann's distribution. [1]

Ans:

Q4. What do you mean by the charge neutrality in a doped semiconductor? Explain with a suitable expression. [2]

Ans:

Q5 If the effective mass of electron (m_n^*) in Si crystal is 0.3m$_0$, find the thermal velocity (V_{th}) of electron in the same crystal at 300 k. [2]

Ans:

P.T.O.

Q6. What is the reason behind the lowering of metal work function in a MS junction under high field application? [2]

Ans:

Q7. What are the criteria for constructing a metal-semiconductor non-rectifying (Ohmic) contact? [2]

Ans:

Q8. How can you define radiative and non-radiative semiconductors? Provide examples for both type of semiconductors. [2]

Ans:

Q9. What is the difference between band to band and Auger recombination for low level injection? Write the expression of carrier life time for both the cases. [2]

Ans:

Q10. Write the expression of multiplication factor in avalanche breakdown and what is the condition for unlimited multiplication? [2]

Ans:

Q11. Why is the reason to maintain equilibrium in semiconductor of a MOS junction under biasing condition? [2]

Ans:

Q12. Draw and label a Q-V characteristic of an ideal MOS junction where n-type Si is used as the semiconductor. Indicate the operating conditions i.e. accumulation, depletion and inversion. [2]

Ans:

Q13. Draw a schematic of a parasitic bipolar transistor formation in an n-MOSFET due to impact ionization effect. Also, show the direction of the flow of electron and hole. [2]

Ans:

Q14. Draw an energy band diagram of a short channel n-MOSFET to show the drain induced barrier lowering (DIBL). [2]

Ans:

Q15. Draw a qualitative I_D-V_{GS} characteristics for p-channel depletion MOSFET. [2]

Ans:

Q16. A small negative voltage is applied to the bulk terminal of a MOSFET (w.r.t the source). Tick the correct answer [2]

- Depletion charge (in channel): Increase/Decrease
- Inversion change (in channel): Increase/Decrease
- Threshold voltage: Increase/Decrease

Q17. Consider ‘s’ is the scaling factor. For, constant field scaling, write the appropriate scaled parameters.
Example: Gate length (L): L/s [2]

- Doping (N_A):
- Propagation delay (τ):
- Power delay product ($P.\tau$):
- Depletion width (W_D):

Q18. Consider a chrome-silicon metal-semiconductor junction where work function of chromium is 4.5 eV and donor doping of silicon is 10^{17} cm^{-3}. [4]

(a) Calculate the barrier height
Ans:

(b) Built-in potential
Ans:

If, 5 V reverse bias voltage is applied to the junction, calculate

(c) Depletion layer width
Ans:

(d) Electric field in the semiconductor at the interface
Ans:

(e) Potential at half of the depletion width
Ans:

(f) Capacitance per unit area
Ans:

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BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

COMPREHENSIVE EXAMINATION

Semester I: 2022-2023

Part B: Open Book

MEL G631: Physics and Modelling of Microelectronic Devices

Date: **27/12/2022** Maximum Marks: **45** Maximum Time: **105 minutes**

Given (Use, if not specified in the questions):
$q=1.6\times10^{-19}$ C, $k=1.38\times10^{-23}$ $m^2kgs^{-2}k^{-1}$, T=300 K, kT/q=0.026 V, $\varepsilon_0=8.85\times10^{-14}$ F/cm
Si: $\varepsilon_r=11.8$, $n_i=1.45\times10^{10}$ cm^{-3}, $E_g=1.12$ eV, $\mu_n=1300$ cm^2/V-s, μ_p(Si)=480 cm^2/V-s, $q\chi=4.05$ eV,
$N_C=2.8\times10^{19}$ cm^{-3}, $N_V=1.04\times10^{19}$ cm^{-3}.
Au: φ_M = 4.75 eV

Attempt all the questions.

Q1. In a given n-p junction donor and acceptor concentrations are 1.45×10^{17} cm^{-3} and 1.45×10^{16} cm^{-3}, respectively. Consider, room temperature (300 k), $\mu_n=1300$ cm^2/V-s, $\mu_p=480$ cm^2/V-s, $\tau_n=\tau_p=1$ µs.

Also consider the physical thickness of n and p both the side as 100 µm.

(a) Sketch and label majority and minority carrier concentrations under 0.6 V forward bias. Also find the value of injected minority carriers at the boundary for both the side. **[4]**
(b) Calculate $I_n(x_p)$, $I_p(-x_n)$ and total current (I) at 0.6 forward bias. Consider cross sectional area of the np junction as 10^{-4} cm^2. **[3]**
(c) Repeat part (a) and calculate $I_n(x_p)$, $I_p(-x_n)$ and total current (I) for the physical thickness of n and p both the side as 1 µm. **[6]**
(d) What is the change in total current for 1 µm device as compared to the 100 µm device? **[1]**
(e) What is the average electron and hole carrier life time of the minority carrier in 1 µm device? **[1]**

Q2

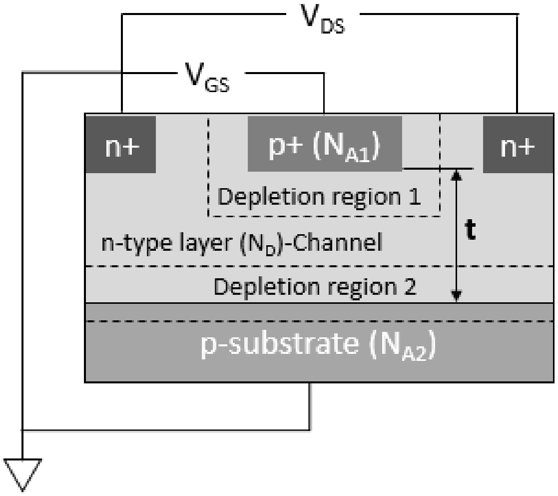
(a). For an n-channel MOSFET derive the following expression for the channel voltage $[V(y)]$ at the edge of saturation (i.e. pinch off). **[6]**

$$V(y) = (V_{GS} - V_T)\left(1 - \sqrt{1 - \frac{y}{L}}\right)$$

Where, L is the channel length (or gate length); source end as y = 0 and drain end as y = L.
(Hint: *Use $I_{DS}=I_{DSAT}$, ignore velocity saturation*)

(b). Consider a long channel n-MOSFET with gate width near source end is W and drain end is W+(L/α) where, L is the channel length and α (>1) is a constant. Derive a drain current expression in linear and saturation region considering gradual channel approximation approach. (Consider: μ_n: Constant mobility and C_{OX}: Oxide capacitance). **[5]**

Q3. A schematic of junction filed effect transistor is shown in the figure below. Consider W and L are the width and length of the device. Derive a drain current expression for very small V_{DS}. **[5]**



Q4. Consider a n–channel n^+ poly-SiO_2-Si MOSFET with gate oxide thickness (t_{ox}) = 5 nm, channel length (L) = 0.6 µm and acceptor density (N_A) = 2×10^{17} cm^{-3}. Calculate V_{DSAT} value with and without gradual channel approximation considering flat band voltage (V_{FB}) as -1.1 V, V_{GS} = 2 V and bulk to source voltage (V_{BS}) as zero. Again calculate the V_{DSAT} considering velocity saturation where saturated velocity of electron at room temperature (V_S) is 10^7 cm/s and electron mobility μ_n = 450 cm^2/V-s. **[7]**

Q5. Consider a n–channel n^+ poly-SiO_2-Si MOSFET with gate oxide thickness (t_{ox}) = 5 nm, channel length (L) = 180 nm and width (W) = 324 nm, acceptor impurity (N_A) = 2×10^{17} cm^{-3} and number of fixed oxide charge 4.92×10^{11} cm^{-2}. Calculate **[7]**

(a) Threshold voltage
(b) Surface potential at V_{GS} = -334 mV
(c) Calculate drain current at V_{GS}= -334 mV considering V_{DS} = 0.5 V and μ_n = 500 cm^2/V-s.
