BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

MID-SEMESTER EXAMINATION

Semester I: 2023-2024

Open Book

MEL G631: Physics and Modelling of Microelectronic Devices

Date: **10/10/2023** Maximum Marks: **60** Maximum Time: **90 minutes**

Given (Use, if not specified in the questions):
$q=1.6\times10^{-19}$ C, $k=1.38\times10^{-23}$ $m^2kgs^{-2}k^{-1}$, T=300 K, kT/q=0.026 V, $\varepsilon_0=8.85\times10^{-14}$ F/cm
Si: $\varepsilon_r=11.8$, $n_i=1.45\times10^{10}$ cm^{-3}, $E_g=1.12$ eV, $\mu_n=1200$ cm^2/V-s, μ_p(Si)=480 cm^2/V-s, $q\chi=4.05$ eV,
$N_C=2.8\times10^{19}$ cm^{-3}, $N_V=1.04\times10^{19}$ cm^{-3}.
GaAs: $\varepsilon_r=12.4$, $E_g=1.424$ eV, $q\chi=4.07$ eV
Au: $\varphi_M = 4.75$ eV
Consider room temperature (300 k) if not mentioned in the question.

Q1. A pn junction, having uniform doping in the p and n sides, is approximated as a linear junction instead of abrupt junction approximation where the charge concentration changes from most positive value (n −type side) to the most negative value (p −type side) in the smoothest possible way as shown in the Figure (a) and (b). In the linear pn junction, charge concentration $[\rho(x)]$ in the depletion layer changes linearly as

$$\rho(x) = -ax$$

Where a is the slope of the linear dependency.

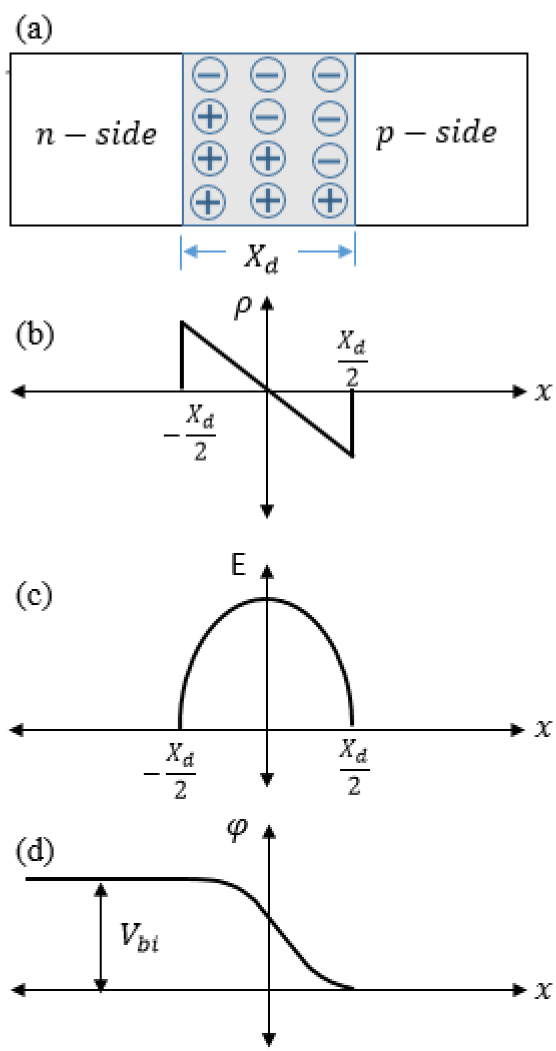
(a) Derive the expression of electric field $[E(x)]$ for the Figure (c). **[5]**

(b) Find the expression of maximum electric field E_{max} at $x = 0$ (Figure (c)). **[2]**

(c) Derive the expression of electric-potential distribution $[\varphi(x)]$ for the Figure (d). **[4]**

(d) Find the expression of built-in-potential (V_{bi}) as shown in the Figure (d). **[2]**

(e) Find the expression of depletion layer width (X_d) as a function of V_{bi}. **[2]**



Q2. For an n-type GaAs/p-type $Al_{0.3}Ga_{0.7}As$ heterojunction at room temperature, ΔE_C = 0.21 eV.

Find the following at room temperature

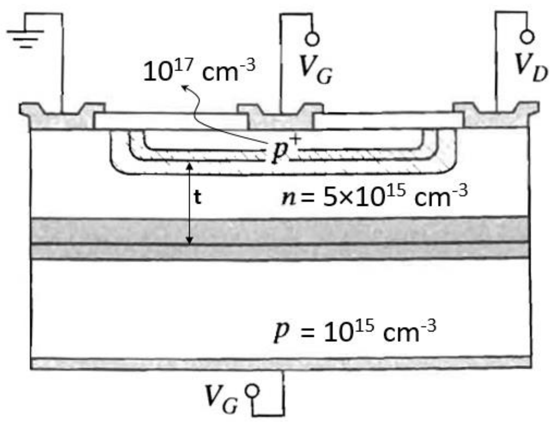
(a) Built in potential to the junction. **[4]**
(b) Total depletion width/depth. **[3]**
(c) Depletion capacitance of the junction. **[2]**
(d) Sketch and label energy band diagram of the heterojunction under equilibrium. **[6]**

Consider, $\chi_{GaAs} > \chi_{Al0.3Ga0.7As}$
GaAs: $N_d = 5\times10^{15}$ cm^{-3}, $N_C = N_V = 7\times10^{18}$ cm^{-3}, E_g = 1.424 eV, dielectric constant = 12.4
$Al_xGa_{1-x}As$: N_a=10^{16} cm^{-3}, $E_g(x)$ = 1.424+1.247x eV, dielectric constant = 12.4-3.12x, N_C=N_V=4.7×10^{17} cm^{-3}

Q3. A Silicon based JFET is biased with V_G voltage to its gate and bulk terminal both as shown in the figure below. If the channel thickness (t) of the FET is 1.5 μm, find the followings

(a) Required minimum V_G to stop the channel at negligibly small V_D. **[7]**
(b) Calculate V_{DSAT} if V_G = -3 V (V_D is significantly high now). **[8]**

[Hint: Use for part (b); $(1+x)^{1/2} \approx 1 + \frac{1}{2}x$, when $x < 1$]



Q4. Consider a n-channel GaAs MESFET has a barrier height (φ_B) = 0.9 V, N_D= 10^{17} cm^{-3}, channel thickness (t) = 0.2 μm, channel length (L) = 1 μm and channel width (W) = 10 μm.

(a) Determine the device is normally on (depletion type) or normally off (enhancement type) and give proper justification. **[4]**
(b) Find the V_{Dsat} value at V_{GS} = 0 V and V_{GS} = -1 V. **[3]**
(c) Find drain current (I_{DS}) and gate terminal current (I_{GS}) when $V_{DS} = V_{DSat}/2$ and V_{GS} = -1. **[4+4]**
(Substrate is connected to ground and ignore depletion region between of n-channel and p-substrate)
GaAs: $N_C = N_V = 7\times10^{18}$ cm^{-3}, dielectric constant = 12.4, $\mu_n=20\mu_p$=8000 cm^2/V-s

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