# BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

COMPREHENSIVE EXAMINATION

Semester I: 2023-2024

**Part A: Closed Book**

**MEL G631: Physics and Modelling of Microelectronic Devices**

Date: **08/12/2022** Maximum Marks: **40** Maximum Time: **90 minutes**

Given (Use, if not specified in the questions):
$q=1.6\times10^{-19}$ C, $k=1.38\times10^{-23}$ $m^2kgs^{-2}k^{-1}$, T=300 K, kT/q=0.026 V, $\varepsilon_0=8.85\times10^{-14}$ F/cm
**Si:** $\varepsilon_r=11.8$, $n_i=1.45\times10^{10}$ $cm^{-3}$, $E_g=1.12$ eV, $\mu_n=1300$ $cm^2$/V-s, $\mu_p$(Si)=480 $cm^2$/V-s, $q\chi=4.05$ eV,
$N_C=2.8\times10^{19}$ $cm^{-3}$, $N_V=1.04\times10^{19}$ $cm^{-3}$.
**Au**: $\varphi_M=4.75$ eV

*Answer should be very brief and to the point.*

Q1. What is the probability of finding of an electron at the conduction band [$f(E_C)$.] of pure Silicon at 20ºC ? [2]
Ans:

Q2. Consider a $P^+n$ junction, where $N_D$ is tripled. If everything else remains same, how do the parameters listed below change. Tick the correct answer. [2]

(a) Depletion capacitance: Increase / Decrease

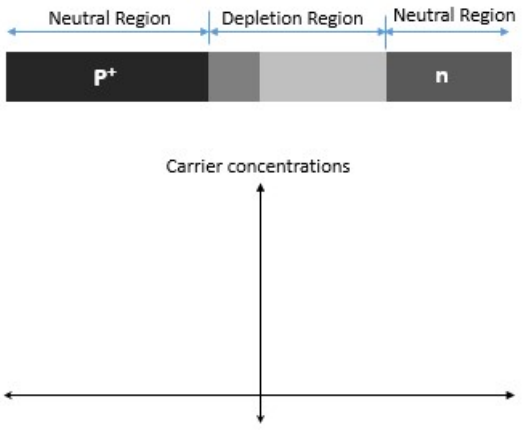
(b) Built-in potential: Increase / Decrease

(c) Breakdown voltage: Increase / Decrease

(d) Ohmic losses: Increase / Decrease

Q3. For a Si p-n junction, $N_A=N_D=10^{17}$ $cm^{-3}$. Find the applied revise bias voltage when maximum electric field will be $5\times10^5$ V/cm. (T = 300 k) [2]
Ans:

Q4. Draw the qualitative distribution of excess minority carriers (i.e. $p_n$' and $n_p$') in $p^+n$ junction. [2]




P.T.O.

Q5 Write the continuity equation for electron while electric filed is constant. [2]
Ans:

Q6. What is preferred for less shift of the threshold voltage due to effect of body bias potential (or body effect). Tick the correct answer. [1]

(a) High/ Low substrate doping ($N_A$)

(b) Thick/ Thin oxide thickness ($t_{ox}$)

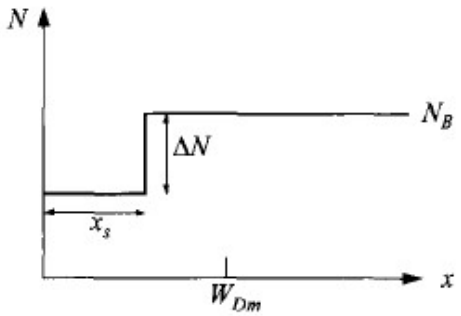
Q7. For a sharp subthreshold slope (small S), what will be the preferable combinations. Tick the correct response: [2]

(a) High / Low channel doping,

(b) Thick / Thin oxide thickness,

(c) High / Low interface-trap density

(d) High/ Low substrate bias voltage.

Q8. 


If the given non-uniform doping profile is used instead of a uniform doping profile for a MOSFET, what will be change in depletion width and threshold voltage. Tick the correct response. [1]

(a) Depletion width will increase / decrease

(b) Threshold voltage will increase /decrease

Q9. Draw a schematic of a short channel MOSFET to indicate the charge sharing effect. [2]
Ans:

Q10. What is the reason behind the faster operation in SOI MOSFET as compared to the conventional bulk MOSFET? [2]
Ans:

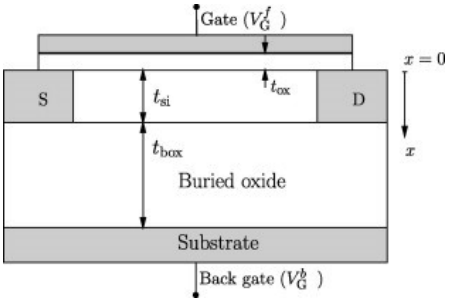
Q11. An n-channel MOSFET having oxide thickness of 4 nm, substrate doping of $5\times10^{16}$ $cm^{-3}$, and flat band voltage of -1.1 V. Calculate the particular gate to source voltage ($V_{gs}$) where immediate oxide breakdown can possible at the starting of strong inversion. (Breakdown strength of $SiO_2$ is 18 MV/cm). [2]
Ans:

Q12. Consider an ideal MOS capacitor having n-type Si substrate. Draw the qualitative carrier (hole and electron) distribution profile under week inversion. Ans: [2]

Q13. Draw an energy band diagram of $SiO_2$/Si system to indicate the band offset of ~3.1 eV. Ans: [2]

Q14. Draw a schematic of floating body in a n-channel partially depleted (PD) SOI MOSFET. Clearly indicate the all the capacitance and pn junction diodes. Ans: [2]

Q15. Sketch and label the transfer characteristics ($I_D$ vs $V_{GS}$) of a n-channel **buried** device (MOSFET). Ans: [2]

Q16. 


Write the expressions of all three capacitances used in threshold voltage expression of the given FD-SOI-MOSFET. [3]

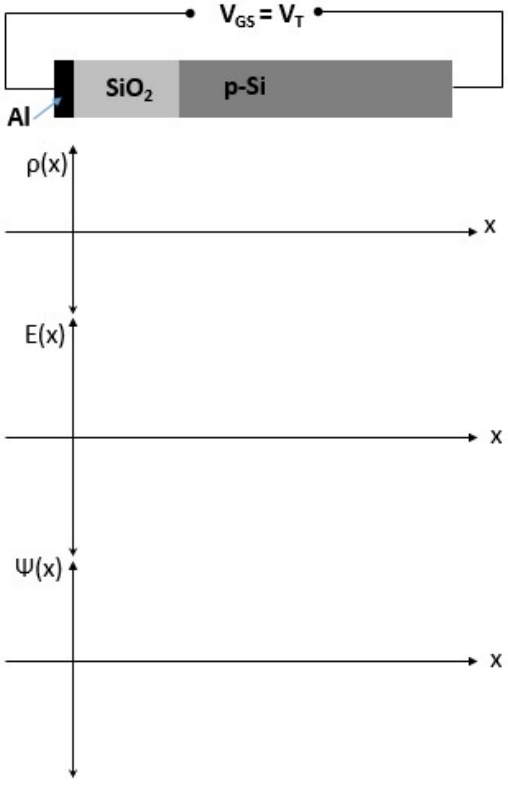
Q17. Consider 's' is the scaling factor. For, constant field scaling, write the appropriate scaled parameters. Example: Gate length (L): L/s [2]

- Doping ($N_A$):
- Propagation delay ($\tau$):
- Power delay product ($P.\tau$):
- Subthreshold slope (S):

Q18. Draw an energy band diagram of a short channel n-MOSFET to indicate the drain voltage induced barrier lowering. [2]

Q19. Draw the $V_{DS}$ vs $V_{GS}$ plot and indicate linear, saturation and subthreshold region. [2]

Q20. Draw the charge (ρ), electric filed (E) and potential (ψ) distribution pattern for the following MOS junction at $V_{GS} = V_T$. Consider the MOS junction is ideal one. [3]

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# BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

COMPREHENSIVE EXAMINATION

Semester I: 2023-2024

**Part B: Open Book**

**MEL G631: Physics and Modelling of Microelectronic Devices**

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$N_C=2.8\times10^{19}$ $cm^{-3}$, $N_V=1.04\times10^{19}$ $cm^{-3}$.
**$SiO_2$**: $\varepsilon_r = 3.9$

*Attempt all the questions.*

**Q1.**

**(a)** Sketch and label the energy band diagram of a Metal-Silicon (M-S) junction under thermal equilibrium at 300 K. Consider, metal work function 4.1 eV, donor doping in Silicon as $5\times10^{16}$ $cm^{-3}$. Comment on the type of the junction. **[5]**

**(b)** Given acceptor profile $N_A(x)=N_0e^{-ax}$. Sketch and label following quantities with respect to 'x'.

(i) Diffusion current ($J_{pdiff}$) **[2]**
(ii) Drift current ($J_{pdrift}$) **[1]**
(iii) Electric filed ($E_x$) **[2]**

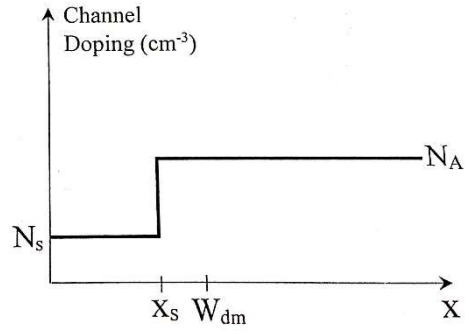
**Q2.** An abrupt $p^+n$ silicon junction (long base) having $10^{-4}$ $cm^2$ cross section with following information

| **$p^+$ side** | **n side** |
|---|---|
| $N_A = 10^{17}$ $cm^{-3}$, $\tau_n = 0.1$ µs<br>$\mu_p = 200$ $cm^2$/V-s, $\mu_n = 700$ $cm^2$/V-s | $N_D = 10^{15}$ $cm^{-3}$, $\tau_p = 10$ µs<br>$\mu_n = 1300$ $cm^2$/V-s, $\mu_p = 450$ $cm^2$/V-s |

At a particular bias, current is measured as 1 mA.

(a) Find the applied bias voltage **[5]**
(b) Find $I_p$ hole current at $x = x_n$ **[2]**
(c) Also, find in (electron current) at $x = x_n$ **[1]**
(d) Sketch the hole and electron current of the $p^+n$ junction under forward bias. **[2]**

**Q3.** Consider an n-channel MOSFET with $n^+$ polysilicon gate. Gate oxide thickness is 7 nm, fixed oxide charge $5\times10^{10}$ $cm^{-2}$ and p-type body has a step (non-uniform) doping ($N_A>>N_S$) as shown in the figure below. Write the threshold voltage expression considering the approximation $N_S \approx 0$ and find the value of $X_s$ and $N_A$ when threshold voltage is 0.3 V and corresponding surface potential ($\Psi_S=2\Psi_B$) as 1 V. Also, calculate the maximum depletion width ($W_{dm}$). **[10]**



**Q4.** Consider interface charges $Q_f/q=5\times10^{11}$ cm$^{-2}$ (applicable for front and back both the interfaces)

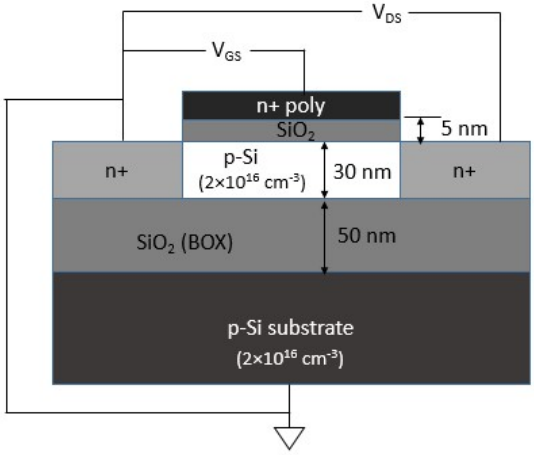
(a) Show the type of the device i.e. FD or PD SOI. **[2]**

(b) Find the back surface potential ($\Psi_{sb}$). Also, comment on the condition of the back interface (i.e. accumulation, depletion or inversion). **[4]**

(c) Find accurate front gate threshold voltage of the SOI MOSFET. **[3]**

(d) Find body factor (n) of the device and estimate $V_{DSAT}$ for applied $V_{GS}$=1 V. **[1]**

*(Hint: Consider the flat band voltage in the calculation)*

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