BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, RAJASTHAN
II SEMESTER, 2022-2023
MID-SEM TEST CLOSED- BOOK (17 MARCH. 2023, 11am-12.30 pm))
MEL G632

TIME - 90 mins. **ANALOG I.C. DESIGN** **MAX. MARKS=25**

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Justify your answers, use only standard symbols. **TOTAL 3 Questions**

NOTE:

- ✓ Symbols have their usual meaning. Answers should be clear, concise and legible. Specify your assumptions clearly.
- ✓ **No marks** for unnecessary theoretical explanations. Marks will be deducted for calculation mistakes.
- ✓ Take (for 0.5 micron technology, assume long channel MOSFET equations are valid)

V_{DD}= 3.3 V, L_{min}=1um

NMOS ---V_{TN}= 0.7V γ= 0.45 $\sqrt{V}$ K'=$\mu_N C_{OX}$= 140 $\mu A/V^2$ λ=0.1 V^{-1}

PMOS---- V_{TP}= - 0.7V γ= 0.4 $\sqrt{V}$ K'= $\mu_P C_{OX}$ = 40 $\mu A/V^2$ λ=0.1V^{-1}

Unless necessarily required or specified in the question.

-assume γ=λ=0 in drain current analysis. Bulk terminal of all NMOS/ PMOS connected to ground/ Vdd ***Assume matching of devices and operating in saturation region wherever required***

Q1. Consider the block level diagram of a 2 stage amplifier with active load circuit shown in **Fig. 1.**

Given = DC current I_B (of stage-1) = 50 uA. Vin = 1.5V+ 5 mV sinwt , Vov= 0.2 V, Vout (DC)=0.7V

Required dynamic specifications of amplifier--- Rin > 100 MΩ, Rout ≤1 KΩ , |Avo| =(vout/ vin) ≥100,

a) Based on data given, write the name of stage-1 and stage-2 of the given amplifier .

b) Sketch and label the complete schematic of the entire circuit. Clearly mark stage-1 and stage-2 in you diagram. Also specify matched transistor pair/s.

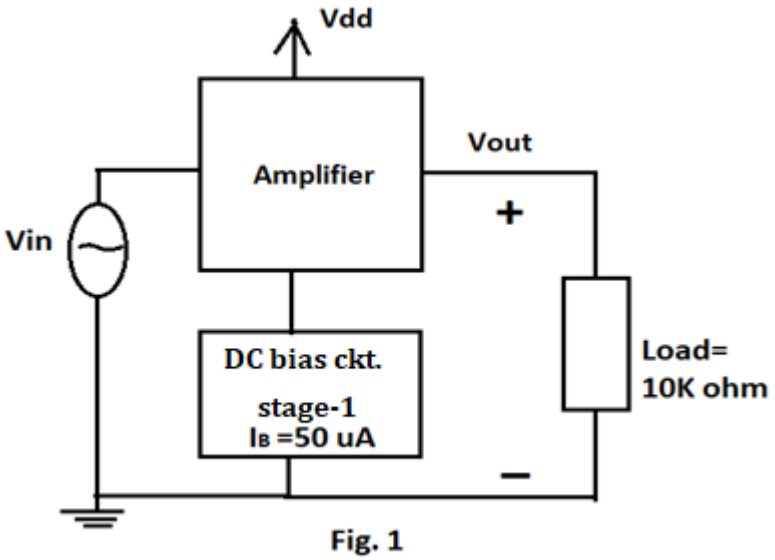

Fig. 1

c) Determine the value of bias current of second stage of amplifier.

d) Write values of DC voltages at every node in circuit of part (b)

e) Determine the value of Av (with load)= (vout/ vin)

[10]

Q2. Consider the circuit shown in Fig. 2 .

Given Vov. = 0.2V . Assume matching of differential arms in the circuit. .

Iss (basic current mirror circuit) = 100 uA= 2 $I_{D,5,6}$

Vid= vin1-vin2= 10 mV sinwt +1.7V,

Vod= vout1- Vout2

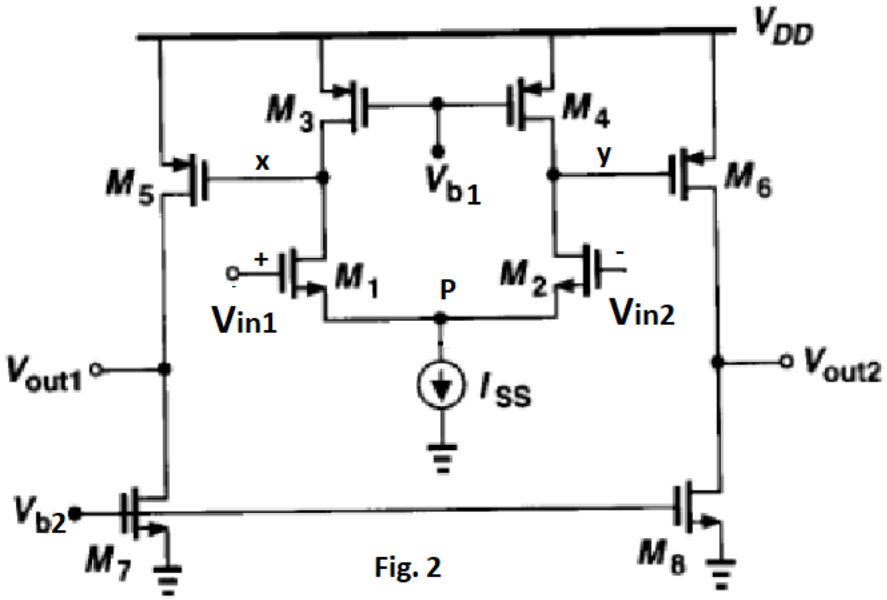

Fig. 2

a) Identify the type of amplifier in Fig. 2

b) Determine small signal voltage gain $\boldsymbol{A_{dm}} = \left(\frac{v_{od}}{v_{id}}\right)$ in dB

c) Modify the following equation , in case of mismatch in differential arms , in terms of differential input only.

Given Input vin1= vin2= vicm remains equal.

$$\boldsymbol{v_{od} = A_{dm}v_{id} + A_{cm}v_{icm}}$$

d) If trans-conductance of only M5 and M6 transistors get 2 % mismatch during fabrication such that $|g_{m5}| \neq |g_{m6}|$. Determine the value of $g_{m,\ nominal}$ and $\Delta\ g_m$

e) For **part (d),** calculate the value of |vod| due to mismatch . Here, assume ro5= ro6 in calculations.

Hence calculate $|Acm|_{diff}$ in part (d). Given Input **vin1= vin2= vicm** remains same.

[12]

Q3. Answer the following. Justify with reason/s .

a) The intrinsic gain of a MOSFET does not change with change in bias current. Why?

b) Source degeneration of a MOSFET increases its dynamic resistance. Why?

c) In cascode amplifier, cascode transistor is replaced by a passive resistor R. Write the voltage gain expression intuitively.

d) What is the significance of figure of merit $\{g_m/ I_D\}$ of MOSFET amplifier

[5]

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