Birla Institute of Technology and Science, Pilani

MEL G632 Analog Integrated Circuit Design

Comprehensive Examination, II Semester 2021-2022

OPEN BOOK

Time: 180 min. **Max. Marks=40** **Date: 12-05-2022**

Total 5 questions.

Unless given specifically

Take -- V_{DD} =3.5V, Lmin= 1 um

For NMOS device $\mu_n Cox = 140\ \mu A/V^2$, $V_T = 0.7$ V , $\lambda = 0.05\ V^{-1}$, Vov=0.2 V.

For PMOS device $\mu_p Cox = 40\ \mu A/V^2$, $V_T = -0.7$ V , $\lambda = 0.05\ V^{-1}$, Vov=0.2 V.

For NPN/ PNP device β=30 V, $V_{CE,SAT}$ =0.2V , V_A=100V, kT/q= 25mV(at room temp.), Is= 10^{-14} A, $V_{BE,ON}$ = 0.6V, $\alpha \approx 1$

NOTE:

If not specified in question ------

- Ignore λ in drain current equation. Neglect body bias effect in calculations
- Bulk of nmos connected to ground and bulk of pmos connected to V_{dd}. Specify your assumptions. Justify your answers.
- Unless specified, assume all MOSFET are biased in active region
- All symbols have usual meaning. Assume matching in the circuit wherever required

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Answer all the sub-parts of a question in sequence and one place only. Clearly show the procedure used to arrive at the answer for full credit. Report the answers with proper units.

Q 1. Answer the following in brief with proper justification--- take current sources as nearly ideal.

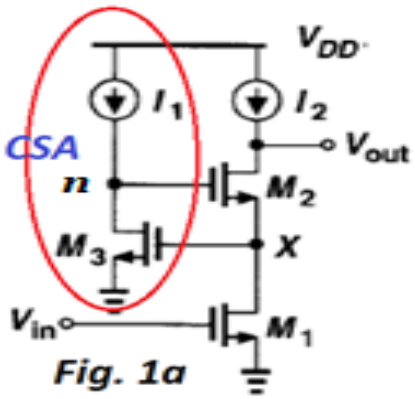
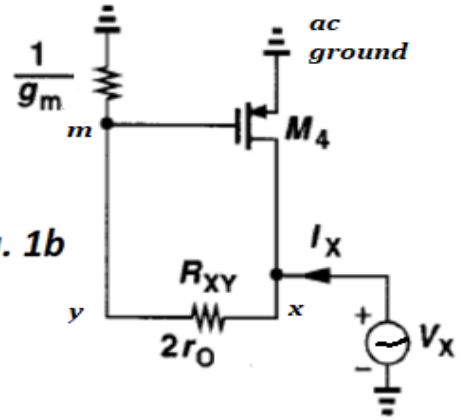


Fig. 1a



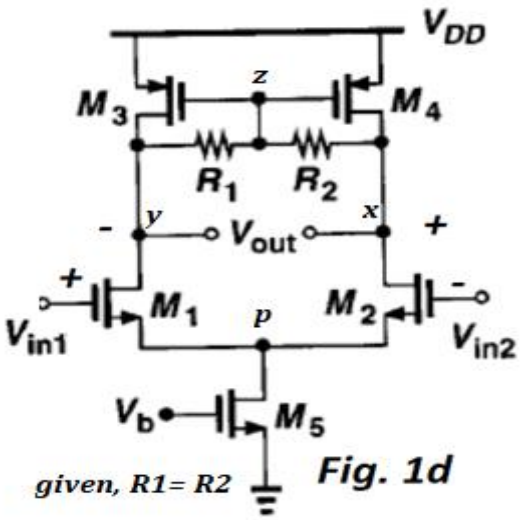


Fig. 1d

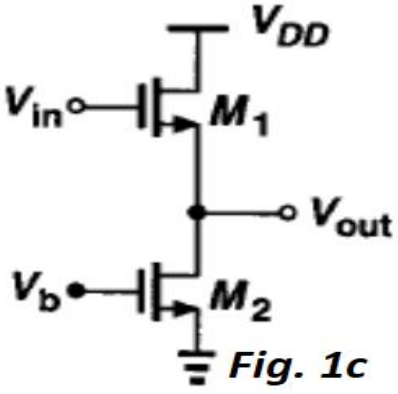


Fig. 1c

P.T.O

a) For Fig. 1a--- determine minimum DC voltage required at node Vout.

b) Re-design the schematic (CSA part) of Fig. 1a to obtain Vout $_{DC, MIN}$ =2 Vov.

c) Derive the expression of [Vx/ Ix] in Fig. 1b

d) In Fig. 1c, Sketch and label ***Vout*** *versus* ***Vin*** as Vin varies from 0 to Vdd. Mark important transition points

e) Intuitively, write the expression for differential mode gain (Adm), and common mode gain (Acm) for Fig. 1d with and without mismatch in R1, and R2 only.

[10 marks]

Q 2. Consider the amplifier circuit given in Fig. 2. All transistors operate in active region. Matched devices-(M2, M3, M4, M5)

Given dc current Iref= I4, Rd ⇒ very large (∞)

a) Determine the value of the intrinsic voltage gain of M1

b) Determine low-frequency small signal output impedance 'Rout' of the amplifier, and dynamic output voltage swing

c) Determine the value of maximum small signal voltage gain (Vout/ Vin) and transit frequency (ω_t) of amplifier. Here, Take Cox= 0.4 pF/um^2.

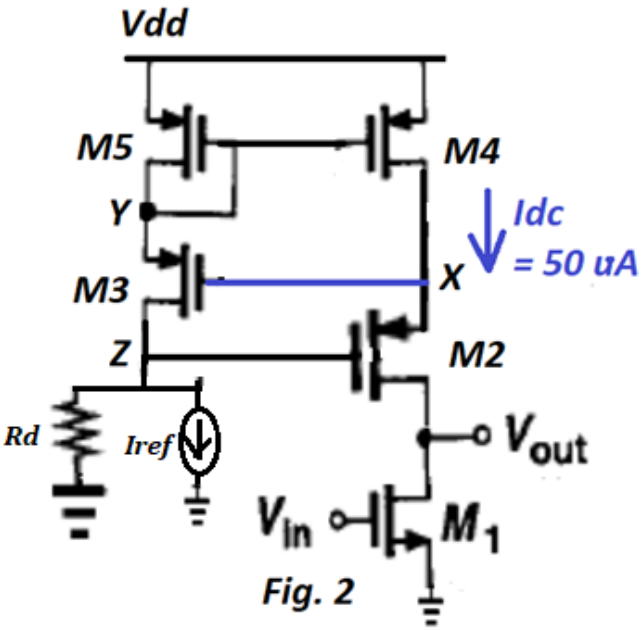


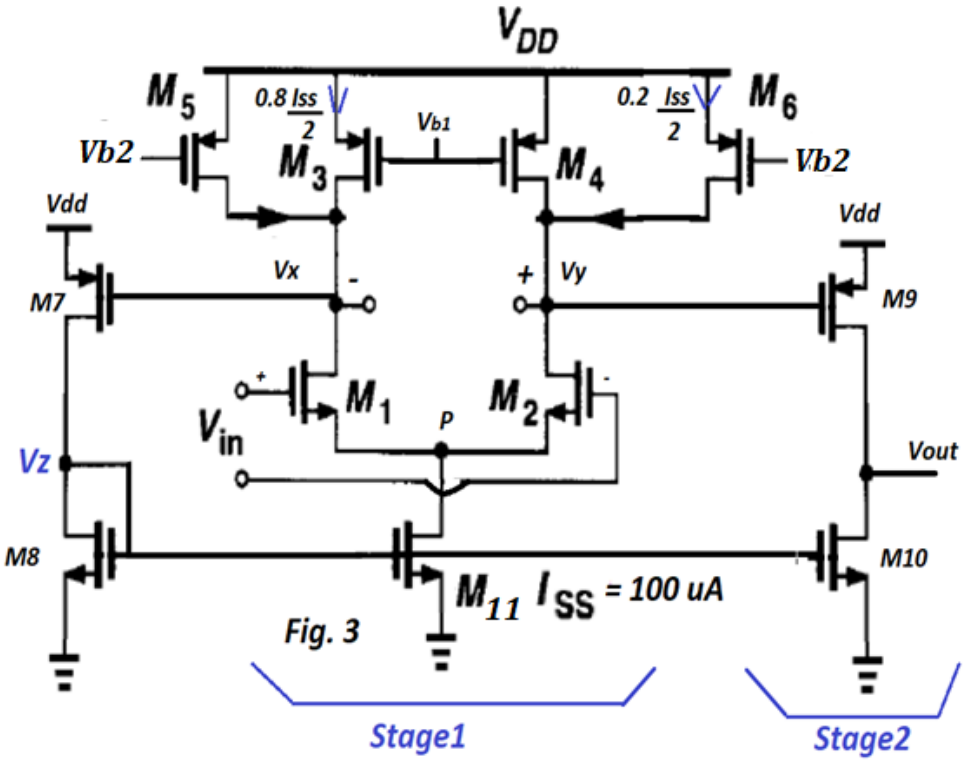
Fig. 2

[8 marks]

Q 3. Consider the circuit shown in Fig. 3. Assume all transistors operate in active region and have Vov.= 0.2 V. I9=I7=75 uA,

At nodes, x and out, given—Cx, y = Cout= 6 pF

Matched Pairs: (M1, M2), (M3, M4), (M5, M6), (M7, M9), (M8, M10)



a) Determine the magnitude of low-frequency ac voltage gain $A_{vo} = \frac{V_{out}}{V_{in}}$ and dc voltage at node Vout.

b) Determine the magnitude of only dominant pole/s and ω_{-3dB}. Hence calculate, gain crossover frequency (Gx). Also, determine if the amplifier is stable or not for maximum feedback closed loop condition. Neglect any non-dominant zero / pole frequency

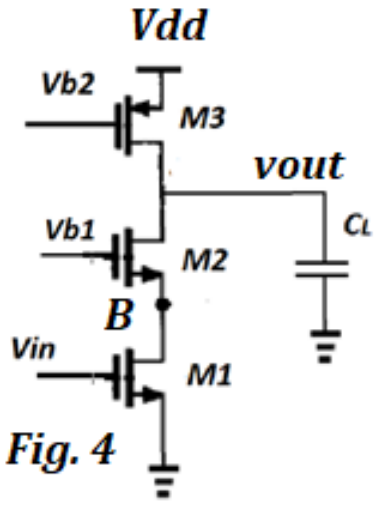
c) Now, determine the value of the Miller compensation capacitor (C_c) required to obtain a phase margin of 60 degrees for maximum feedback closed loop condition.

[15 marks]

Q 4. In Fig. 4,

a) Identify all capacitances (including parasitics) that will appear at node Vout. Hence, write the expression of complete **Cout.**

b) Modify the circuit of Fig. 4 to generate a negative capacitance at node Vout to reduce pole frequency at node Vout. While modifying, ensure not to change low-frequency voltage gain.



[4 marks]

Q 5. Design a common mode feedback circuit (CMFB) for the amplifier of Fig. 5 to obtain dc voltage at node Vx, y = 1.8 V.

a) Sketch and label the complete circuit with CMFB in place.

b) Determine the required dc current through (M5, M6) (with CMFB circuit in place) for the loop to be stable with Gx < 1000 rad./ sec. Here take load capacitor C_L = 5 pF value present at the output/s of the circuit.

[5 marks]

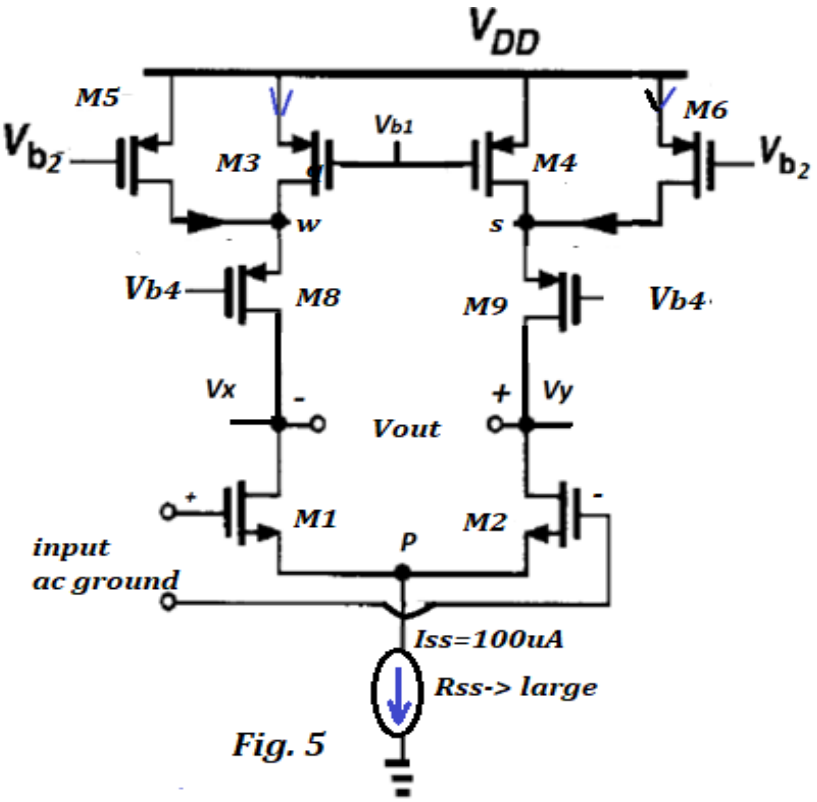


Fig. 5

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