Birla Institute of Technology and Science, Pilani
II semester 2017-2018

MEL G641- CAD for IC Design (Midsem Test) -- Closed Book

Date: 05.03.2018 MM: 30 Duration: 90 Min.

Note: **Solve all part of a particular question together in sequence.**

Q1: For the following VHDL code, draw the waveform for signals X, Y and Z1 up to 24 ns when input 'Z' is changed to logic '0' at time 5 ns. **(4 M)**

```
entity LMN  is port (Z: in bit:='1'; Z1: out bit:='1');
end LMN;

architecture LMN of LMN is
signal X,Y: bit:='1';
begin
```

```
process (Z)
begin
if Z='0' then
X<= '0' after 4 ns,'1' after 6 ns,'0' after 8 ns, '1' after 12 ns;
Y<='0' after 2 ns,'1' after 8 ns,'0' after 12 ns, '1' after 15 ns;
Y<='0' after 6 ns,'1' after 9 ns,'0' after 12 ns, '1' after 15 ns;
Z1<= X OR Y  after 3 ns;
end if;
end process;
end LMN;
```

Q2 : In a hierarchical design an entity XYZ is used as a sub-module to design a top module having entity name as TOP. The entity TOP has three architecture namely PQR1, PQR2 and PQR3. A entity XYZ also has three architectures namely ARCH1, ARCH 2 and ARCH 3. Now write a configuration which binds architecture PQR2 to entity TOP, it also binds architecture ARCH 2 to the all the instances of entity XYX within the entity TOP. (Assume default binding rules wherever applicable). **(2 M)**

Q3: For the circuit shown in figure 1, find the test vectors to determine (i) SA1 fault at node 'H' (ii) SA1 fault at node 'K' (iii) Bridging fault between 'I' and 'E' such that both node are at logic '0' ? **(3 M)**

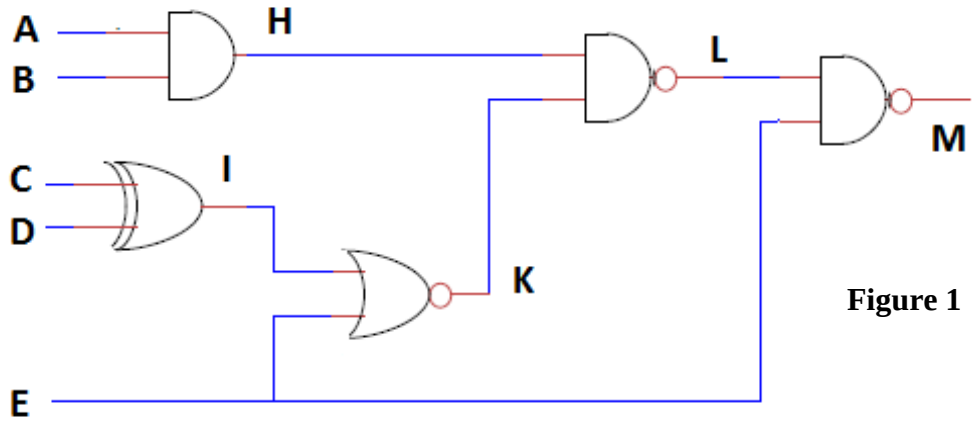

Figure 1

Q4: (i) For the circuit shown in figure 1 mark the all timing levels. Assuming equal high to low and low to high propagation delay time of gates calculate the maximum and minimum arrival times at node 'Y' for the case when input arrival time = 0 ns.
(Given: Gate and wire delays in ps are: wire delay = (50:80:100), AND2= (200:240:300), NAND = (160:200:240), XOR= (240:280:320), NOR = (200:250:300). (Consider wire delays and assume same wire delay for fanout cases) **(3 M)**

(ii) The circuit shown in figure 2, shows the network of combinational logic (CL) where CL2 use results obtained from figure 1 (including all wire delays) and D-flip flops/ Register. The minimum logic contamination delay ($T_{logic,\ cd}$) and maximum logic propagation delay ($T_{p,\ logic}$) are indicated in the figure. Assuming the all positive edge triggered flip flops with $t_{clk\text{-}q}$=50 ps, t_{setup}=40 ps and t_{hold}=60 ps then calculate maximum clock frequency for sequential circuit to operate correctly and check for any hold violations for following cases (i) Clock is ideal i.e. no skew and no jitter. (ii) The difference in clock arrival between any two flip flop is ±75 ps. (Ignore all visible wire delays in figure 2.) **(4 M)**

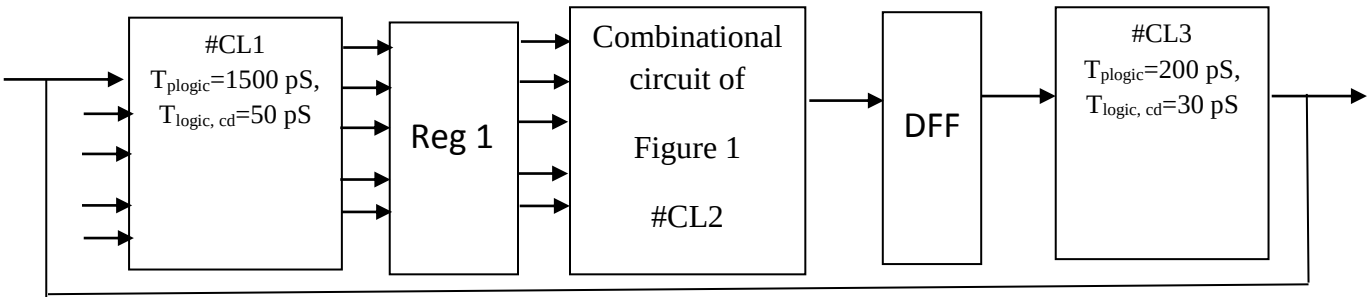

Figure 2

Q5: For the following VHDL codes draw the schematic circuit diagram of expected circuit behavior. **(4 M)**

```
entity LMN is
port (A,B,C,CLK: in bit;D,E: out
bit);
end LMN;
architecture LMN of LMN is
signal
T1,T2,T3,T4,T5,X1,X2,X3,X4:bit;
begin
process (A,B,C)
begin
X1<=A xor B; X2<=A and B;
X3<=B and C; X4<=A and C;
end process;
```

```
process
begin
wait until CLK='1';
T1<= X1;
D<=T5 xor T1;
T2<=X2;
T3<=X3;
T4<=X4;
T5<=C;
E<=T2 or T3 or T4;
end process;
end LMN;
```

Q6: Write the expected synthesis output for the following Verilog code. **(2 M)**

```
module ABC (x5,x4,x3,x2,x1);
output x5,x4;
input x3,x2,x1;
reg x5,x4;
always @(x3,x2,x1)
  begin
    if (x1)
      x4 =x3 ;
    else
      x5 = x2;
  end
 endmodule
```

Q7: Answer the following questions in brief (write only important points).

(A) List the disadvantages of ASIC based digital designs. **(1 M)**
(B) List the several EMI noise in a digital system and also list the different layout techniques to reduce such problem. **(2 M)**
(C) In the Hardware software co-design list the blocks used for the software processing? **(1 M)**
(D) Explain the need of Isolation Cells in Low Power VLSI Design process? **(1 M)**
(E) Which graphics format is preferred for CAD system and why? Also list the different coordinate sets used by the graphics package? **(2 M)**
(F) Briefly explain the liberty format that used to compute the cell delay? **(1 M)**

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